Silicon Light Emitting Devices for Integrated Applications

Le Minh Phuong

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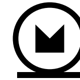

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SILICON LIGHT EMITTING DEVICES FOR INTEGRATED APPLICATIONS

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SILICON LIGHT EMITTING DEVICES
FOR
INTEGRATED APPLICATIONS

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
prof. dr. F.A. van Vught,
volgens besluit van het College voor Promoties,
in het openbaar te verdedigen
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door

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geboren op 30 oktober 1974
te Hanoi, Vietnam

Dit proefschrift is goedgekeurd door de promotoren
Prof. dr. H. Wallinga
Prof. dr. ir. A. van den Berg

en de assistent promotor
Dr. J. Holleman

"… the wise man looks into space, and does not regard the small as too little, nor the great as too big; for he knows that there is no limit to dimensions…"

~Lao-Tse~

To my parents,
my sister Thanh Truc,
and my wife Thuy Ha

PREFACE

Light emission from silicon has received growing interest in the past decades. The main reason is the possible integration of light emitters with silicon chips, which would add significantly new functionalities to the modern ICs, e.g. the optical interconnects are being investigated as an outstanding solution to the interconnects bottleneck posed by conventional metal lines. Next, in the field of silicon-based sensors and actuators, a silicon light source would be prime for realizing reliable, inexpensive and high yield devices.

This thesis brings up new facts on the integration capability, photochemistry, and properties of the prototype devices based on the light emitting diode antifuse. The chapters are arranged with increasing level of sophistication. The fist chapter also reviews the current trends of the research on silicon light emitting devices. The last chapter extends the reach of the thesis to two new types of devices, which emit efficient near infrared photons.

The work presented in this thesis is the result of four years' work by the author, carried out at the Semiconductor Components Laboratory, MESA$^+$ Research Institute, University of Twente. It has been four years that seems to pass by incredibly fast. It is four years of joy, delight, sadness, homesick as well as many other positive and negative feelings. They, however, have been along with the completion of this work. The thesis would of course be impossible without help and guidance from many colleagues and friends. I would like to acknowledge with gratefulness to all of you who have supported by one way or another. My heartily thanks are to specifically dedicate to:

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Last but most beloved, thanks are to my wife Thúy Hà for her love and faithfulness to me. Her presence during the completion of the thesis has made such a difficult task much less stressful. *You are wonderful, darling!*

During the preparation, a lot of efforts were made to make this thesis a good piece of work, however small errors and mistakes are unavoidable. I would appreciate very much any report from you. Finally, I hope you have the courage to go through the thesis!

Enschede, 26 December 2002

Le Minh Phuong

LIST OF ACRONYMS

μTAS	Micro Total Analysis System
AFM	Atomic Force Microscopy
BJT	Bipolar Junction Transistor
BOX	Buried OXide
BPSG	Boron Phosphor Silicate Glass
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
CV	Capacitance Voltage
DBR	Distributed Bragg Reflector
DILED	DIslocation loop engineering Light Emitting Diode
DPROM	Diode Programmable Read Only Memory
EL	ElectroLuminescence
FIB	Focused Ion Beam
FN	Fowler Nordheim
FWHM	Full Wide at Half Maximum
HDS	Highly Doped Substrate
IC	Integrated Circuit
ITO	Indium Tin Oxide
JFET	Junction Field Effect Transistor
LATODE	LATeral diODE
LDS	Lowly Doped Substrate
LED	Light Emitting Diode
LPCVD	Low Pressure Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MiCS	Micro Chemical System
ONO	Oxide Nitride Oxide
PCE	Power Conversion Efficiency
PL	PhotoLuminescence
PLICE	Programmable Low Impedance Circuit Element
SEM	Scanning Electron Microscope
SIMOX	Separation by IMplanted OXygen
SiRN	Silicon Rich Nitride
SOI	Silicon On Insulator
SRH	Shockley Read Hall
TDDB	Time Dependent Dielectric Breakdown
TEM	Transmission Electron Microscope
TMAH	Tetra Methyl Ammonium Hydroxide
UV	UltraViolet
VLSI	Very Large Scale Integration

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Chapter I

INTRODUCTION

This thesis is dedicated to the study of an IC-compatible light emitter for sensor and actuator applications, particularly in integrated micro-chemical systems. Nanometer-scale light emitting antifuses have demonstrated to be a candidate regarding efficiency, size, and fabrication ease. IC-compatible means that the device is realized on silicon wafers with silicon technology.

In this introductory chapter, a few vital points about silicon are discussed which clarify why it is difficult to enhance light emission in silicon material. It is also argued why a silicon light emitter, fabricated with silicon technology, is very much desired. Secondly, different approaches and successes (to some extent) by groups worldwide on making light sources in silicon are briefly described. The following section is the motivation that has triggered this research. The structure of the thesis is explained in the final section.

I.1 Introduction

I.1.1 Crystalline silicon material

Physical [1]

Silicon crystallizes in the diamond structure, which consists of two interpenetrating face-centered cubic lattices displaced from each other by one quarter of the body diagonal. In semiconductors with zinc-blende structure such as GaAs, the Ga and As atoms lie on individual sub-lattices, thus the inversion symmetry of Si is lost in III-V binary compounds. This difference in their crystal structures underlies the dissimilar electronic properties of Si and GaAs.

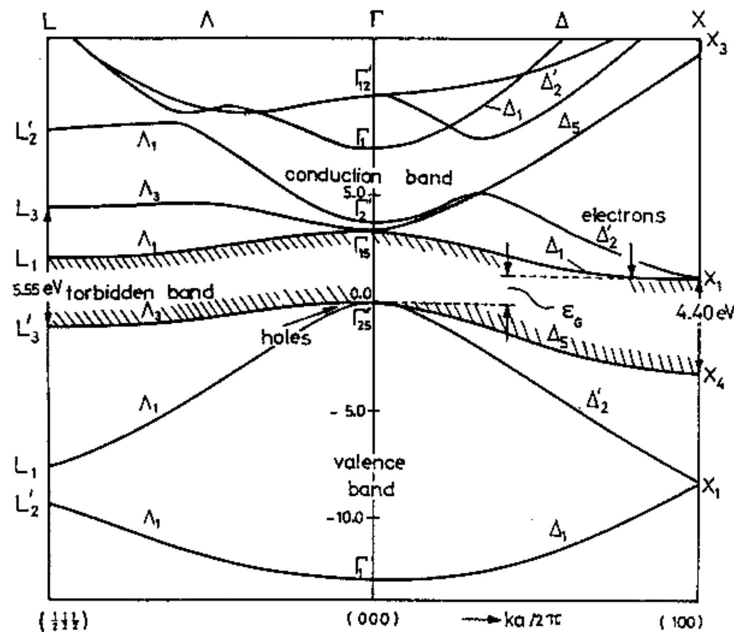

Figure I.1-1. Dispersion relations for the energy *E(k)* of an electron or hole versus wave vector length in the first Brillouin zone of silicon (after [2])

The energy band structure, in semiconductor in general, and Si particularly, is derived from the relationship between energy and momentum of a carrier, which not only depends on the crystal structure but also on the bonding between atoms, their respective bond lengths, and the chemical species. The band structure is often quite complex and can only be calculated theoretically. Figure I.1-1 shows the dispersion relations for the energy *E(k)* of an electron

or hole for wave vector length in the first Brillouin zone [1]. *E(k)* has maxima or minima at the Brillouin zone center and zone boundary symmetry points, but additional extremes may occur at other points in the Brillouin zone. The valence band structure is much the same for many semiconductors and exhibits a maximum at the Brillouin zone center or Γ point (i.e. at *k=0*). In the case of Si the lowest point in the conduction band occurs away from high symmetry points near the X point at the Brillouin zone boundary (along <001>). The bandgap of Si is the difference between this point and the valence maximum at point Γ. Because these two states have difference wave vectors, Si is termed an indirect bandgap semiconductor.

On the other hand, in GaAs the minimum in the conduction band occurs at Γ point which means that the transition can take place directly at *k*=0 between initial and final states having the same wave vector. The electron-hole radiative recombination in Si can only occur if momentum is conserved, that is, the excited electron wave vector must be reduced to zero. This, in pure Si, happens via the transfer of momentum to a phonon that is created with equal and opposite wave vector to that of the initial state in the conduction band. Such a two-step process has a low probability compared to direct gap recombination. This is why Si is such a poor light emitter.

Semiconductor carrier transitions [4]

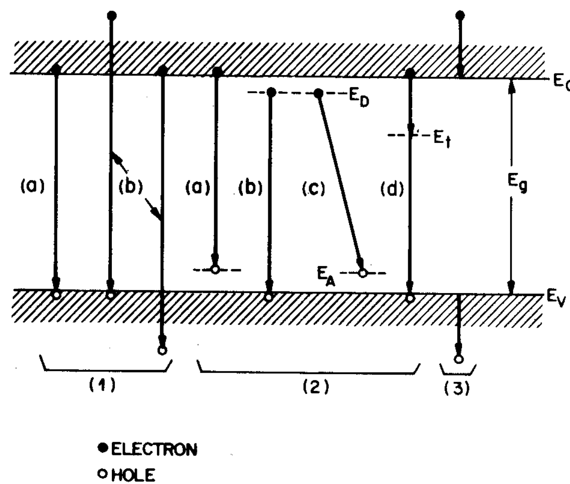

Figure I.1-2. Basic transitions in a semiconductor (after [3])

The radiation of photons in semiconductors is generally accomplished by the recombination of carriers across the bandgap. The transitions of carriers, in both direct and indirect energy bandgap semiconductors, can be classified as follows. The first category (1) is the interband transition: (a) intrinsic emission corresponding very closely in energy to the band gap, where phonons or excitons may be involved, and (b) higher energy emission involving energetic or hot carriers, sometimes related to avalanche emission.

The second classification (2) is the transition involving chemical impurities or physical defects; (a) conduction band to acceptor, (b) donor to valence band, (c) donor to acceptor, and (d) deep levels.

The third class (3) is the intraband transition involving hot carriers, sometimes called deceleration emission or Bremsstrahlung [2].

I.1.2 Benefits of silicon optoelectronics

Photodetectors, waveguides, wavelength demultiplexers and modulators have all been realized in silicon-based technology [5][6]. Solving the problem of low efficiency of silicon-based efficient light emitters would greatly expand the use of silicon as an optoelectronic material. Direct integration of optoelectronic devices into microelectronic circuitry with single CMOS processing would effectively reduce the manufacturing costs and increase yields. That is because of the avoidance of expensive and exotic compound semiconductor technologies. Furthermore, "If an all-silicon laser could be created it would revolutionize the design of supercomputers and lead to new types of optoelectronic devices…" [8].

I.1.3 Requirements and potential applications

The general requirements in Si-based light sources are efficient light emitting diodes, lasers, and optical amplifiers for use in optical communication technologies such as fiber optics or displays. Operating wavelengths in the range of 0.45 − 1.6 μm (2.8 − 0.7 eV) are needed to cover both full color displays and fiber optics operating wavelengths of 1.3 and 1.55 μm.

Specific applications for such sources include fiber optic transmitters, optoelectronic interconnects within and between computer chips, optical controllers for phased-array microwave antennas, information display screens,

printing elements in xerography, and writing and read-out of optical compact disk information [1].

In an emerging field of research and development, Micro Total Analysis System (μTAS), which is backed by silicon micro-technology, optical absorption sensors are widely utilized for chemical analysis. This sort of application imposes relatively less constraints on the light emitter requirements. It was the initial idea in the beginning phase of this research to search for a suitable silicon-based light source for applications in μTAS.

I.2 "engineering light out of silicon" up-to-date

It has been exposed that an efficient light emitter in silicon will broaden the spectrum of products from silicon semiconductor industry. Such a light emitter might extend the application of silicon as the size limits are approached. A review on the development of this topic would contribute a great deal to the philosophy of this thesis. Therefore, in the second part of the first chapter, we summarize the current approaches, and promising achievements by different research groups. The classification is established rather on the technological strategies, including nanoscalization, incorporation of other elements, and machining modification.

I.2.1 Nanoscalization

Porous silicon

The structural and luminescence properties of porous silicon were reviewed vigorously in [10]. This form of silicon material has received enormously intensive study since the proposal in 1990, which claimed efficient visible light emission out of high porosity structures arose from quantum confinement effects. The main optical characteristics of porous silicon material are:

- The emission color can be tuned by the pore sizes. Prior to obtaining efficient luminescence, some "threshold" porosity had to be exceeded. With 70–80% porosity, there is a rapid rise in photoluminescence (PL) intensity and a pronounced blue shift of the PL peak.

- Surface chemistry of the pore has profound effect on PL intensity, PL spectra, degradation and the emission quenching process of the material.

- External PL efficiencies as good as 1% have been achieved. The reason for the good PL efficiency is not that Si has become a direct gap semiconductor but rather that the crystallites are defect-free and well passivated [11].

In [12], an effort was made to integrate porous LED devices with transistor circuitry. External power efficiency 0.1% and 1MHz modulation bandwidth were achieved. However, this is just a proof of concept [7], more improvement is needed, in particular the stability and reproducibility. The lower efficiency of electroluminescence (EL) compared to PL is attributed to the difficulty of carrier injection from the contact into the porous Si, and the poor transport properties of porous Si. The low mobility of carriers in porous Si is reasoned for the slow switching behavior. The emission line width of this particular porous Si-LED is rather broad (>100meV); hence an integrated optical cavity would be necessary. The potential advantage of such a device lies in the possible integration with microelectronic circuitry, though the incompatible fabrication method by anodization and the mechanical integrity still need further improvement. Many research programs were stopped, however, due to the difficulty of obtaining stable devices.

Nanocrystal

Optical gain in silicon material, in nanocrystalline form, was reported for the first time in [13], signaling the feasibility of a future true silicon laser [9]. The densely packed nanocrystals of 3nm in size were embedded in thermal silicon dioxide grown on silicon wafers by ion implantation and thermal annealing. The nanocrystals formed a thin layer just below the surface of the matrix material. The finding was explained by a population inversion of radiative states associated with Si/SiO_2 interface. The authors suggested that their gain was a consequence of the high quality of the silicon nanocrystal-oxide interface, which has many 'surface states' that emit light per nanocrystal.

Consequently [8], Canham has figured out why optical gain had never been seen in porous silicon that makes the stringent difference between these two

forms of nanoscale structures. The luminescence process of un-oxidized porous Si does not involve the surface states, and is very dependent on the size and shape of the nanocrystals. On the other hand, Pavesi [13] claimed that very good quality SiO_2 and Si nanocrystals were needed to observe the interface level, which in other Si-based systems, e.g. porous Si, is hindered by interfaces with defects or the low quality of the oxide.

I.2.2 Hybrid approaches

Iron silicide [15]

The first EL device was made and reported in [14]. The approach used was to incorporate direct-gap iron disilicide in a conventional silicon p–n junction diode to provide a route for direct radiative recombination. Carrier injection is achieved conventionally under forward bias. Therefore, the iron disilicide was introduced at the recombination region adjacent to the p-type side of the depletion by means of implantation of Fe ions (dose 1×10^{16} cm^{-2}). The implantation energy was chosen to place the peak of the precipitate distribution above the depletion region of the silicon p–n junction. The isolated precipitates produced on annealing are single-crystalline β-$FeSi_2$. EL measurement shows a peak at 1.54 μm, but the intensity sharply decreases as temperature increases from 80K to room temperature. The quantum efficiency was estimated to be around 0.1%.

This approach is simple and straightforward. It is a direct solution to fiber optic communication with silicon-based emitters. However, the efficiency still needs to be improved to about one order of magnitude larger. To do that, the dispute over the nature of the band gap: direct or indirect, should first be worked out, though photo-luminescence at a wavelength of 1.5 μm has been observed in this material and has been argued to be band-edge-related luminescence from the β-iron disilicide.

Europium Silicate

In 1999, J. Qi et al. reported the "Electroluminescence of europium silicate thin film on silicon"[16]. The light emitting active layer was a 2-μm thick, RF-sputtered europium silicate film sandwiched between two electrodes, a p-type silicon substrate and top transparent ITO layer. The material analyses indicate that the silicate film is a uniform film of nanocrystals (sizes of 9 nm)

containing $EuSiO_3$ and $EuSiO_4$. Although oxygen took up 61% in relative concentration of the film, its origin was not clear. Injected carriers bound at the europium centers recombine and give energy to Eu^{2+} ions. These ions consequently emit light through the $(4f)^6(5d)^2$–$(4f)^7$ transition. Europium silicate is an insulator, thus a large voltage is required for the EL. The external quantum efficiency was also estimated at 0.1%. The spectrum shows a peak at 560nm, and a broad structure covering nearly the complete visible range (400-800nm). Modulation of the EL signal was succeeded up to one MHz and probably limited there by the fluorescent decay time of the Eu^{2+} ions.

The advantage of this device consists of potential display applications due to possible large area uniformity and simple fabrication. It suffers the same disadvantage of low efficiency, μs switching time, not to mention the high operational voltage of a few tens of volts.

Erbium doped [17]

Implantation of erbium in different matrix materials is the main fabrication method for incorporating this rare earth element, which emits a standard telecommunication wavelength at 1.54 μm by Er^{3+} intra-4f transitions. In crystalline silicon, the equilibrium solid solubility of erbium is so low that non-equilibrium concentration is necessary. EL devices were fabricated with an emission peak at 1.535μm; in reverse bias breakdown, emission was far more efficient than in forward bias. The mechanism of emission in reverse bias was impact excitation of Er^{3+} by accelerated electrons across the junction. Much more details on the electroluminescence of erbium-dope silicon is found in [18], where it was concluded that optimization of the role of the ligands, such as oxygen or fluorine, in the excitation and back transfer processes, through band-gap states, crystal field engineering or coupling to the lattice, would be the pathway to increase the quantum efficiency.

I.2.3 Micro-engineering

Dislocation loop arrays

In this VLSI compatible approach [19], boron implantation was used to simultaneously create a p-type doing region as well as dislocation loops. These loops are supposed to introduce a local strain field, which modifies the band structure and provides spatial confinement of the charge carriers. This elegant

approach implies a strategic idea, which aims at reducing the efficient non-radiative recombination route and enhancing the radiative one. The EL spectrum peaks around 1.13–1.16 μm. The intensity increases up to room temperature, which is a remarkable advantage over other silicon light emitting systems. This was explained again by the spatial localization of radiative carrier population that is confined and separated from any temperature dependent non-radiative process, thus luminescence quenching is eliminated. This device also has 0.1% quantum efficiency, but according to the author, the efficiency can be improved to comparable value of compound semiconductor LED device.

This bare silicon approach, on the one hand, does not give an optical fiber wavelength which is a disadvantage, but on the other hand, if its response time goes to the *ns* regime instead of presently tens of *μs*, the device will be capable of short range interconnect regime or on chip interconnection.

Solar cell technology

Making use of textured solar cell technology, a breakthrough in improving efficiencies of silicon LEDs has been recently achieved by M. Green [20]. The improved devices were diodes with a special arrangement of junction location to reduce non-radiative recombination rate, and texturing the device top surface with inverted pyramids, formed by anisotropic etching to expose (111) crystallographic planes to increase the absorption of weakly absorbed wavelengths. The latter is the major contribution to the improved performance of the device. According to their report, the device is most efficient at 200K but still gives approximately 1% power conversion efficiency at room temperature. The emission peak follows the temperature dependence of the silicon bandgap.

I.2.4 Summary

It goes without saying that a lot of progress has been achieved in the pursuit for a true silicon light emitter. Many obstacles have been tackled, especially the improvement of emission efficiency. Solutions to fiber optic silicon light sources have also been dealt with, though a silicon-based display seems more likely in the near future [16]. The orientation of the research ahead will probably focus on a fast switching device so that high frequency modulation is possible, in combination with higher efficiency; these favor a silicon laser.

I.3 Nanometer-scale light emitting diode antifuse [21]

The light emitting diode antifuse is a spin-off from its predecessor – the linear antifuse – that was employed in Programmable Low Impedance Circuit Element (PLICE)[22]. It is fabricated by electrically induced breakdown of a thin insulator layer sandwiched between two electrodes. This approach was also further investigated in Diode Programmable Read Only Memory (DPROM)[23]. The distinguished difference of light emitting diode antifuse is the heavily doped electrodes that effectively lowers the threshold voltage for photon emission.

As previously mentioned, the objective of this research, proposed in 1998, is to investigate different properties of nanometer-scale light emitting diode antifuse, purposely aiming at applications in Micro Total Analysis System (μTAS). This device has the advantages of tiny size, low power consumption, CMOS compatibility, and simplicity. The thesis contributes to the scientific understandings of this device on the following aspects.

Source that is small in size

The physical size of the antifuse strongly depends on the capacitor size, the insulator thickness (silicon dioxide in this case), the oxide quality, and the programming procedure. The magnitudes of the programming currents are likely to influence the quality of antifuse rather than the physical size (chapter II).

Higher efficiency

Due to the tiny size of the antifuses, a very high current density could be achieved at the junction, which mediates the higher probability for optical transitions. Small sizes also mean easier collection of emitted photons due to the confined spatial distribution (chapter III).

Compatibility

The antifuse device is entirely fabricated with a CMOS-compatible process on silicon material. For research purposes, simple device structures are manufactured with two masks.

Sensor, actuator and μTAS

Emitting light within entire visible range (wavelengths of 400 to 900 nm), the device under operation can be seen with the naked eye in semi-dark condition. The intensity of near UV photons images itself on the UV sensitive photoresist. Proposed applications of this device were in sensor and actuator fields and would be demonstrated in chapter IV, V, and VI of this thesis.

I.4 Thesis outline

In this thesis, properties and possible applications of nanometer-scale light emitting diode antifuses have been studied. The understanding of electrical properties, electroluminescence, and structure of the diode antifuses have been enhanced, along with the clearly proven applications in the field of sensors and actuators. The avalanche breakdown emission, however, has limitations in further efficiency improvements because it involves the multiplication of carriers and a threshold voltage. The efficiency of the active silicon light emitters is therefore another subject discussed in the end of this thesis.

In *chapter II* the fabrication, structure and electrical properties of the antifuse are discussed. The simple capacitor structures, which are the semi-manufactured devices for antifuses (later called pre-device), can be easily fabricated. The formation and final form of the antifuse device is exposed with destructive methods such as selective etching and Transmission Electron Microscopy (TEM). The electrical behaviors are measured with deliberate comparison to standard silicon diode.

Chapter III is dedicated to the discussion on electroluminescent properties of the antifuse. The spectra of the emission has been recorded and modeled. The emission in forward bias of the lowly doped substrate devices is also mentioned with some interesting facts.

In *chapter IV*, ultra-violet emission from the antifuse is utilized for conduction of a photochemical process. CMOS standard photoresist has been the medium for the demonstration of photochemical reaction. It is also proposed as a reliability testing method based on this phenomenon.

Chapter V deals with a demonstration of an integrated silicon system called silicon opto-isolator. The system consists of a light emitting diode antifuse and photodiode detector. The structure gives an overall electrical efficiency of 1.10^{-6}, which is a clear evidence of improved performance of light emitting diode antifuse compared to other breakdown emission silicon devices.

In *Chapter VI*, the enhanced version of the device discussed in the previous chapter is described. The integrated channel sandwiched between the emitter and the detector transforms the system into a novel microfluidic device with capabilities of a microchemical system, e.g. controlling or catalyzing chemical reaction in the hollow channel with the antifuse, and detecting the process with the integrated detector. Experiments on the channel have been carried out e.g. the influence of the channel medium has been detected on the signal from the emitter.

Chapter VII demonstrates two approaches to the efficiency improvement of the silicon light emitting process in forward bias. The devices fabricated have shown quantum efficiency comparable to that of primitive compound semiconductor LEDs. The possibility of fast modulation of the silicon emitter can be implemented thanks to the fabrication on Silicon-On-Insulator (SOI) wafer, explicitly the suppression of slow carriers diffusion.

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Chapter II

THE DIODE ANTIFUSE

The fabrication of diode antifuses and its formation by electrical fusing and programming is described. The diode antifuse is researched on two main aspects: the electrical properties and the morphology. It is proven that the breakdown in our samples is mainly hard oxide breakdown. The antifuse junction shows improved quality with higher power programming current. The reverse breakdown mechanism mixes both Zener and avalanche. Destructive methods such as selective etching and Focused Ion Beam combined with Scanning and Transmission Electron Microscope have been used to investigate the physical structure of the antifuses.

II.1 Introduction

An antifuse is a conductive link with a size in the nanometer range created by electrical breakdown between two electrodes separated by a thin dielectric. The creation of an antifuse is by fusing, which uses charge to breakdown Fowler-Nordheim tunneling current to stress the oxide. The antifuse being investigated in this research is fabricated from thin oxide capacitors with oppositely doped polycrystalline and/or monocrystalline silicon electrodes and has properties of a diode.

In CMOS technology, oxide breakdown is an important process reliability subject because it limits the yield and reliability of circuits. In consensus, the oxide breakdown phenomenon has been attributed to the positive charge build-up in the region near the injecting, cathode interface. The source of the positive charge is different for the thick and thin oxide thickness regimes [1].

This fusing method has been utilized in the fabrication of Programmable Low Impedance Circuit Element (PLICE) [2] and Diode Programmable Read Only Memory (DPROM) [3]. It has offered significant improvements in size and performance of those devices. Using this technique, the creation of small structure, approaching nanometer range, is possible. The main advantage of this electrical fabrication procedure is its technological ease and simplicity. Semi-manufactured devices are created with CMOS technology on standard wafers that allow mass production.

As it is an unconventional way of device fabrication, the technique also suffers from a few drawbacks. The devices that are made by this technique have a quality dependent on the pre-device (the capacitor), namely the oxide quality, the "weak spots" introduced during manufacturing. These could lead to the difficulty to control the formation of the antifuse. The sizes of the antifuses may be different giving discrepancy in other properties. The location of the discrete device is not predetermined within the size of the pre-device. Thus the relative localization of antifuses, especially light emitting antifuses, is desired in order to bring them into applications.

In this research, the fusing technique demonstrates itself as a new technical approach. The technique can be used for fabrication of both optical and thermal antifuses. The research brings new and interesting knowledge but it is

obviously a challenging work. This chapter will first discuss the fabrication of the antifuses. Their electrical properties and morphology are treated in the followed sections respectively.

II.2 Antifuse fabrication

Device realization details

First, the so-called pre-device, which are silicon dioxide capacitors, had to be produced [5]. They were realized on lowly ($10^{16}cm^{-3}$) and highly ($10^{19}cm^{-3}$) doped p-type silicon substrates. First of all, a layer of 60 nm SiO_2 called field oxide for isolation purpose was thermally grown. Active areas of different sizes were then opened by the first photolithography step and etching. In these areas, a thin oxide of 6 to 8 nm was thermally grown in diluted oxygen ambient (O_2:N_2=1:7) for 4 min at 900°C. To form the top electrode, a 300 nm thick poly-silicon layer was deposited in a Low Pressure Chemical Vapor Deposition (LPCVD) tube. This layer was subsequently implanted with P^+ at 50 keV, at a dose of $8.10^{15}cm^{-2}$. The implanted phosphorus was activated at 900°C for 30 min in a furnace in a N_2 ambient. The devices made on lowly doped substrate were fabricated purposely as a reference.

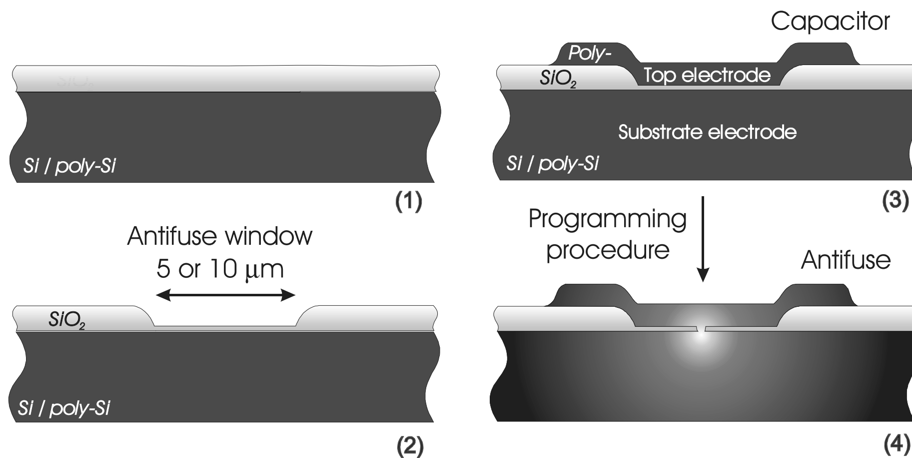


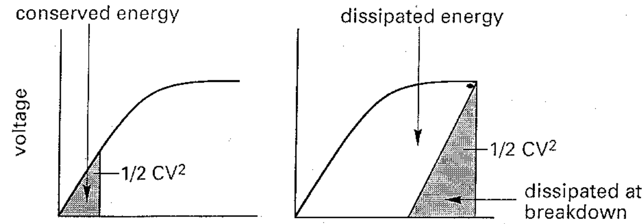
Figure II.2-1. Fabrication process of a simple antifuse

The following capacitor structures for antifuses were realized and studied:

- Polysilicon/ SiO_2/ monocrystalline Si (chapter II, III, IV)
- Polysilicon/SiO_2/ polysilicon (chapter V, VI)
- Poly GeSi/SiO_2/ monocrystalline Si (chapter II)

Programming procedure

Oxide breakdown is named after the method used to bring about the breakdown. Charge to breakdown (Q_{bd}) was employed in our research. A fixed current ($|I_s| = 1\mu A$) is forced through the oxide in the Fowler-Nordheim tunneling regime and the voltage is monitored. When the voltage suddenly decreases, the oxide is considered to have failed. The dissipated power at breakdown is the energy for the formation of the link (right picture, after [4]). Discharge of the parasitic capacitance from the measurement setup was controlled through a 1MΩ series resistor (Figure II.2-2) connected close to the probe needle to ensure low power breakdown [5]. When the gate has negative bias, it is called "gate injection", and thus "substrate injection" for negative bias on the substrate. Subsequently, predetermined post breakdown programming currents I_p, which are larger then the initial discharge currents during breakdown, were applied to stabilize the link structure by heating it up to the melting point of silicon.



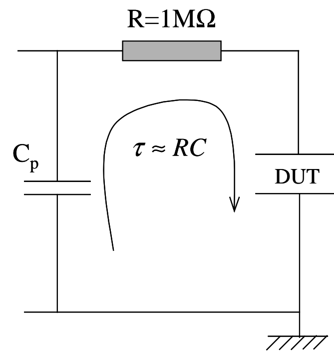


Figure II.2-2. Controlled breakdown setup

The antifuses have been formed on the previously mentioned three structures. Figure II.2-3 below displays their respective spectra. It is obvious that tiny light emitters can be easily fabricated on structures with different materials. However, if antifuses can be created in combination with a direct bandgap material on a silicon wafer by IC compatible processing, it may find immense applications given that the quantum efficiency is improved.

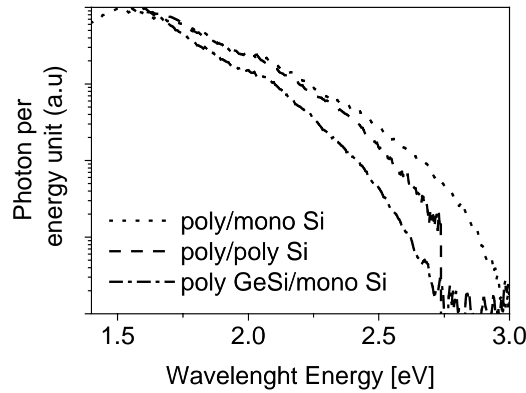


Figure II.2-3. Emission spectra of different structures

II.3 Electrical properties

II.3.1 Pre-device characterization

The quality of oxides can generally be assessed by a few characteristic measurements, such as capacitance voltage method (CV)(Figure II.3-1), voltage ramp, constant voltage stress (TDDB), and charge to breakdown …[9][10]. For charge to breakdown method, a condition for antifuses to be realized with reproducible properties is a high quality oxide that conforms to hard breakdown within a narrow range of Q_{bd} $\left(Q_{bd} = \int_0^{t_{bd}} I(t)dt \right)$.

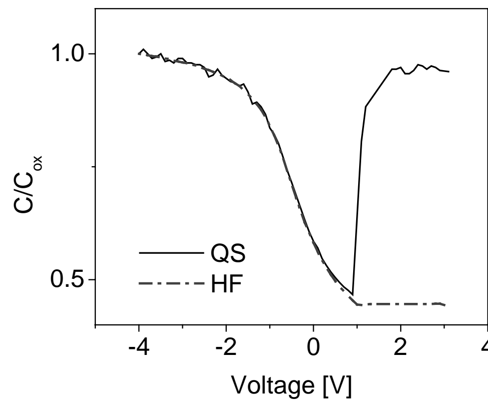


Figure II.3-1. Capacitance-voltage characteristic of a highly doped substrate capacitor, t_{ox}=5.6nm

The gate injection regime produces only a non-linear resistance antifuse (Figure II.3-2 right (a)). Substrate injection, on the other hand, produces diode-like post-breakdown link. This could be explained by the fact that the discharging power in the substrate injection regime is much larger than that in the other case. The dissipated power was enough for an antifuse with rectifying characteristic to form without a further programming procedure. However, this mode was not employed because it is fairly not controlled and degrading the quality of the fuse oxide layer that often produce more than one breakdown link.

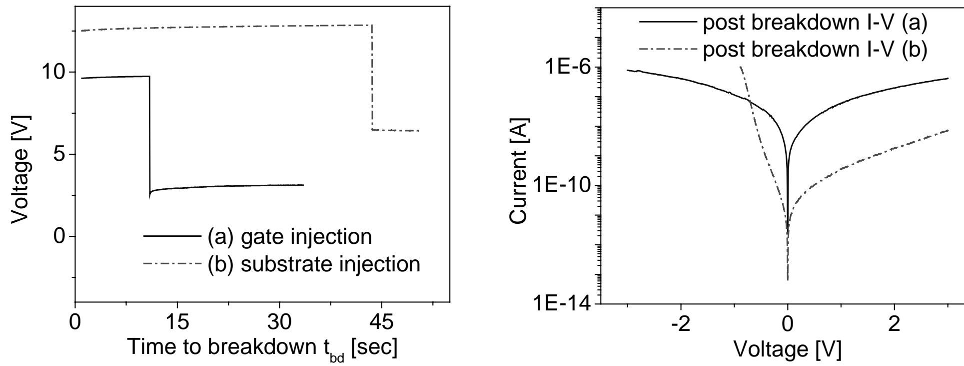


Figure II.3-2. Time to breakdown $|I_s| = 1\mu A$ (left), post breakdown current voltage curves (right); gate injection regime (a), and substrate injection regime (b)

In Figure II.3-3, we plot a post-breakdown resistance value of the breakdown link against the discharging energy. The R_{bd} and ε_{disc} have been defined according to reference [6]

$$R_{bd}[\Omega] = \frac{0.5[V]}{I_{bd}[A]} \qquad \varepsilon_{disc} = S_{cap} C_{ox} \left(V_{gi}^2 - V_{gf}^2 \right) / 2 \qquad (1)$$

In which, S_{cap} - capacitor size, C_{ox} - oxide capacitance, V_{gi}, V_{gf} - instant voltages prior and post to the breakdown respectively. The relationship, of the form $R_{bd} \sim \varepsilon_{disc}^{-m}$, proves that hard breakdown is the dominant occurrence. This conclusion was drawn based on the fact that soft breakdown regime would give a random distribution when plotted on this graph [6].

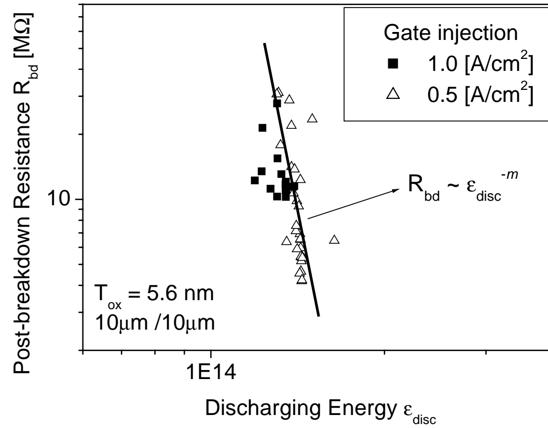


Figure II.3-3. Post-breakdown resistance R_{bd} versus discharging energy ε_{disc}

II.3.2 Antifuse current voltage characteristics

Junction quality

As discussed in section II.3.1 gate injection is used for creating the breakdown. The antifuse is then formed with a programming procedure. It is shown in this subsection that the quality of the antifuse junction is comparable to that of a standard manufactured highly doped p^+-n^+ junction. The reverse leakage currents are in the nanoamperes range. The junction ideality factor *m* [8] $\left(J_f \sim \exp\left(qV/_{mkT}\right)\right)$ has been calculated to be around 2.2 for devices programmed with $I_p = 10mA$.

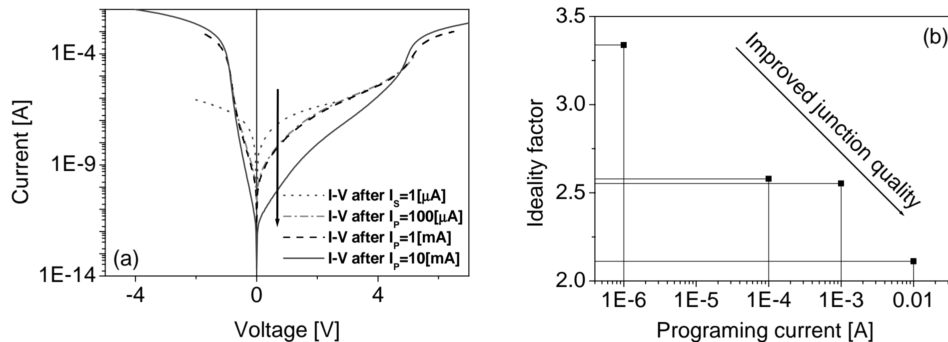


Figure II.3-4. I-V characteristics measured after each programming current; arrow indicating less leakage at higher programming currents (a); Junction quality by ideality factor calculation (b)

In Figure II.3-4 (a) and (b), it is clearly seen that with higher programming current (more power), the leakage current largely decreases which is a significant indication of the improved junction quality [8]. Due to the tiny size of the link, the current density can be extremely high up to 10^8 A/cm^2 and the melting of material at the link can be reached. The opening in the oxide will act as the geometrical size of the antifuse diode, and current flows only through this opening. The real junction where n-type silicon meets p-type silicon is hard to determine. It depends very much on the diffusion of impurities during the melting stage. However, the active region for radiative recombination is supposed to confine closely to the location of the oxide breakdown.

Temperature dependent characteristics

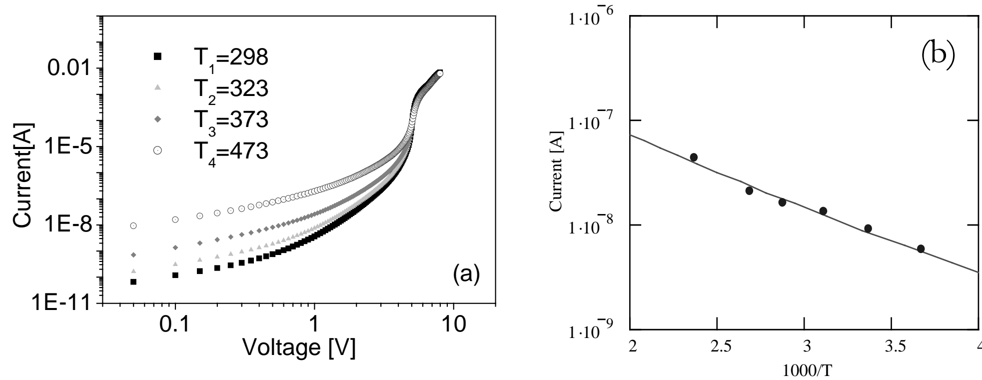


Figure II.3-5. Diode antifuse temperature dependent characteristics of the reverse current (a); reverse current at V_r=1V versus substrate temperature (b), straight line designates the temperature dependence of intrinsic carrier n_i, the activation energy for the leakage current is 0.55 eV

For a silicon diode, a space charge region extends in reverse bias. The increase of the leakage current is due to the generation of electrons and holes within the depletion region. The main processes that take place through intermediate level centers are only emission processes [11]. The diode antifuse resembles that of a standard junction. In Figure II.3-5(a), the temperature dependence of the reverse currents is shown. It is clear that temperature does not influence much the breakdown voltage, which implies a mixed breakdown mechanism, i.e. both Zener tunneling and avalanche breakdown are present.

Furthermore, this can also be confirmed because the breakdown voltage (V_B =5.3V) lies between $4E_g/q$ and $6E_g/q$ [8]. The temperature dependence of the reverse current has the same dependence as the intrinsic carrier concentration n_i which highlights the increased role of generation mechanism with higher temperature $I_{gen} = \frac{qn_iWA_J}{2\tau_o}$ (q –electronic charge, W– junction depletion width, τ_o–effective lifetime within a reverse-biased depletion region, and A_J– cross-sectional area of the junction).

II.4 Antifuse morphology

Due to the destructive nature of the fusing technique, it is important to understand the structure of the resulting device subsequent to its formation. The mechanism of thin silicon dioxide capacitor breakdown, as mentioned in a previous section, is sophisticated. The understanding of this phenomenon is essentially based on statistical approach. The complication grows with the thinner dielectric layers. To this specific case, a simple approach by using different imaging techniques has been implemented. The particular results give a physical image of the event.

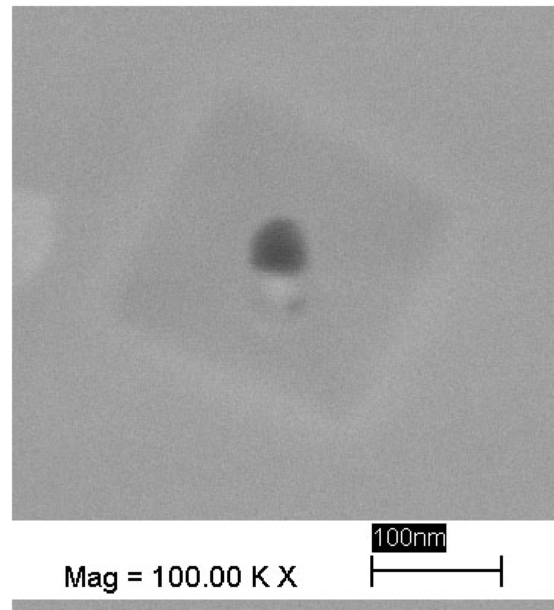
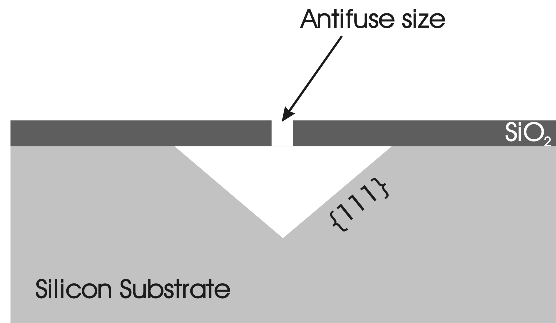


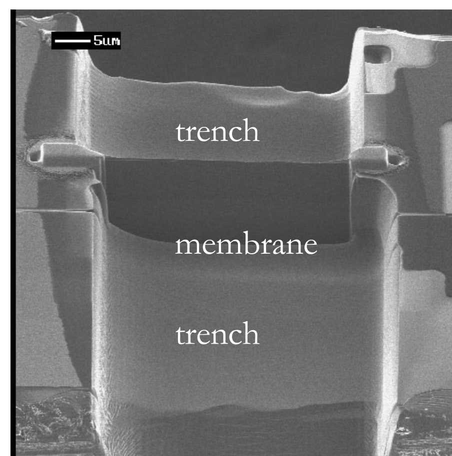
Figure II.4-1. Image of the antifuse size in the thin oxide observed by SEM (oxide thickness 5.6nm, programming current 10mA) after TMAH etching; the light gray square around the darker hole is due to the etching of Si along the {111} planes

Selective etching with TMAH for SEM



The size and shape of an antifuse can be determined by selective etching between silicon and silicon dioxide. If silicon can be etched very selectively, the opening in the oxide can be preserved so that measurements for antifuse sizes are possible. Selective dry etching using Chlorine radicals has been used for gate dielectric breakdown spot determination [13]. The advantage of this technique, claimed by the author, is that Cl^- radicals do not etch SiO_2, which allows very high selectivity. However, comparable selectivity can be obtained much easier with wet etching using TMAH (Tetra Methyl Ammonium Hydroxide) solution. The tuned concentration and temperature of the TMAH solution to obtain the best Si/SiO_2 selectivity ratio has been reported in [14]. For this experiment, our sample was etched in a 10-wt% (weight percentage) TMAH solution for 10 min, at 60°C and which corresponds to an oxide etch rate of 5nm per hour. This slow etching on oxide guarantees almost no damage to the morphology of the feature. The Scanning Electron Microscopy (SEM) is then used to image the sample (Figure II.4-1).

TEM image



For TEM observation [15], a membrane of less than 100nm thick must be produced. Our sample of the antifuse structure was prepared by Focused Ion Beam (FIB) technique. First, the specimen piece containing the region of interest was shaped with a dicing saw. The sample was then glued on a grid by conductive paste. This was later mounted onto the stage of the FIB system. FIB operation is begun when the pressure reaches 10^{-5} mbar or better. As the antifuse was created by electrical means, the location of the antifuse would be random within the capacitor square of $10\times10\mu m^2$. The exact location of the

antifuse was determined by photoresist imaging (chapter IV). A thin line of platinum (Pt) is then selectively deposited across the feature location for protection reason. Next, high beam currents are used to mill trenches on either side of the Pt line. The membrane is obtained by successive fine cuts with less ion beam current. The specimen can then be transferred to the Transmission Electron Microscopy (TEM). Figure II.4-2 shows a poor quality example of the programmed antifuse device. An opening in the thin oxide is clearly seen and the material around this opening has been molten. The oxide layer is deformed and pushed towards the anode. This can only be explained by further investigation, however it is clear that as the molten volume cooling down deformation is induced in the structure.

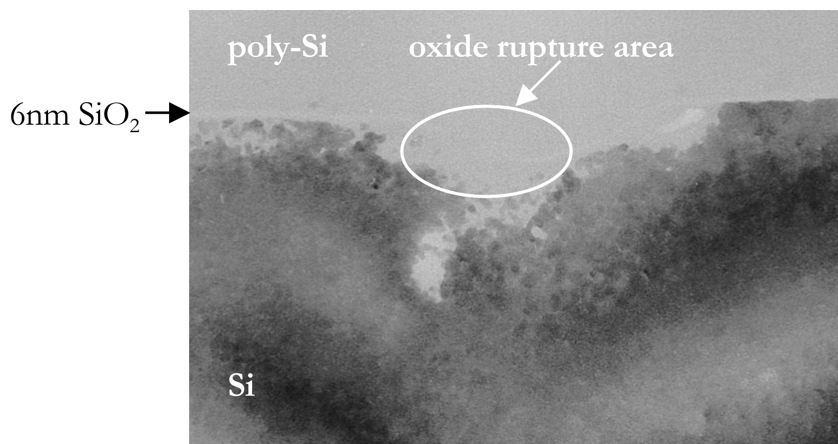


Figure II.4-2. TEM micrograph of a highly destructive breakdown area

Discussion

An antifuse structure postulated here is similar to the structure model proposed in reference [12], which published the first TEM micrograph of programmed antifuse on oxide nitride oxide (ONO) dielectric stack. The programming current produces a sufficiently high temperature to melt the silicon and the dielectric over a small volume centered at the point of breakdown. The dielectric film breaks up into a loose network and protrudes towards the anode, probably due to either the drift momentum of the electrons in the molten silicon or the ejection during the recrystallization process.

The sketch is further supported by the realization of poly-GeSi [16] gate antifuses with a spectrally resolved spectrum displayed in Figure II.4-3. The argument is established on the fact that the large direct energy gap of indirect bandgap materials correlates with the radiative direct interband recombination mechanism [16]. The distinct difference in the high-energy region of the emission spectrum of this antifuse compared to the silicon antifuse evidences the role of Ge in the photon generation process; explicitly the bandgap energy of the material in the emissive region has changed due to incorporation of Ge. The lower energy cutoff in Figure II.4-3 indicates that the antifuse was formed with GeSi properties. The more incorporation of Ge in Si, the smaller the direct bandgap is [16].

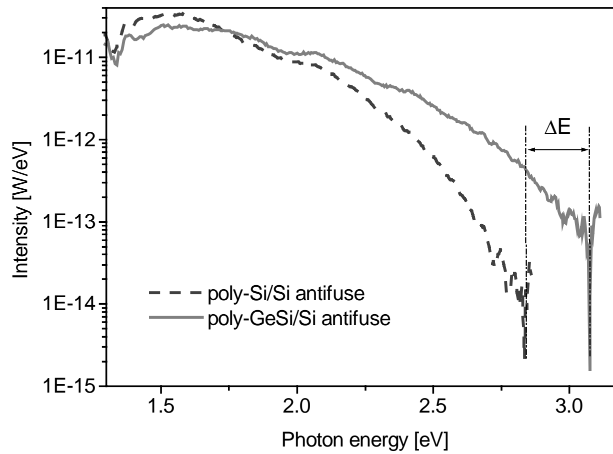


Figure II.4-3. Comparison of Si antifuse and GeSi antifuse spectra

II.5 Conclusions

Diode antifuses have been fabricated and characterized. It is proven that hard oxide breakdown is the main occurrence in these samples. The electrical properties of the antifuses are comparable to conventional silicon diodes. It has been shown that the structure of the antifuses is fundamentally a tiny link formed at the location of the oxide breakdown. The quality of the device is strongly dependent on the power of the programming currents. The reverse breakdown mechanism mixes both Zener and avalanche. Destructive techniques such as selective etching and Focused Ion Beam (FIB) have been used to image the morphology of antifuse structure.

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Chapter III

ELECTROLUMINESCENT NANOMETER-SCALE DIODE ANTIFUSE

Electroluminescent spectra of nanometer-scale diode antifuses were measured in reverse and forward bias. A previously published multi-mechanism model for light emission under avalanche condition from a conventional silicon p-n junction is applied to fit the electroluminescence (EL) spectra for reverse-biased silicon diode-antifuses [10]. The results show that the light emission from reverse-biased diode antifuses under breakdown is caused by the same phenomena as in conventional p-n junctions. Forward-bias spectra of the diode antifuses show different shapes when lightly or highly doped p-substrates are used, but both show a maximum intensity in the infrared region. The forward biased EL intensity in the visible wavelength range of a lightly doped p-substrate is increased by about two orders of magnitude compared to a highly doped substrate device. This visible emission is attributed to the Fowler-Nordheim tunneling current through the SiO_2*, enabled presumably by electron capture at* SiO_2 *trap levels and intraband transition of hot electrons injected into the Si bulk.*

III.1 Introduction

The desire for integration of efficient light emitting devices onto Si-based chip has been readily explained in chapter I of this thesis. Optical sensors & actuators, inexpensive optical displays and high speed optical interconnections are the potential applications. The low efficiency of the photon emission, due to the indirect bandgap of silicon, limits the development of silicon light sources. Research has been carried out to tackle this problem. Yet there is, at present, not a simple way to integrate efficient light sources with silicon microelectronics. More investigation is therefore necessary for the realization of truly efficient silicon-based light emitters.

In this chapter, we investigate and explain the origin of emitted light from nanometer-scale diode antifuses. Due to the small dimensions, an antifuse behaves as a point source with moderate power consumption. At the same time, the CMOS compatible fabrication makes antifuses suitable for large scale integration. The EL spectra from reverse and forward-biased diode-antifuses were measured over the photon energy range 1.35 – 3.2 eV. A multi-mechanism model for avalanche light emission from conventional silicon p-n junction [10] is employed to fit the reverse bias spectra from diode-antifuses under avalanche breakdown condition. The origin of the infrared and visible light emitted in the forward bias mode is also discussed.

III.1.1 Light emission from silicon p-n junction

Forward bias

Forward bias by the application of an external voltage (with positive sign to the p-region) causes the mutual injection of carriers into the majority region of the opposite carrier type within the range of the characteristic diffusion length. This is the mode of operation of all commercially available LEDs and lasers. In silicon diodes, the involved two-step phonon assisted radiation process limits the quantum efficiency to very low value ($\sim 1.10^{-6}$) [4] and is consequently called phonon-assisted emission. The measurement of the emitted spectrum requires a highly sensitive spectrometer. The spectrum features the bandgap wavelength emission around 1.12 eV (1106.25 nm). The line width of this band-to-band recombination characterizes the energy distribution of the injected carriers.

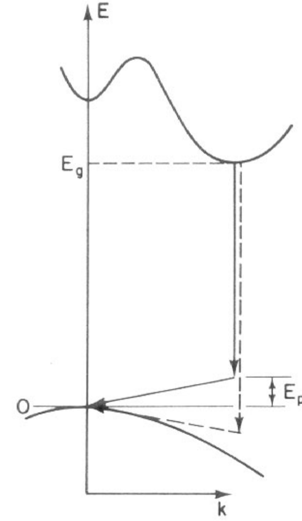

Figure III.1-1. Radiative indirect transition, solid arrows show the photon emission process with a phonon emitted, dashed arrows show the photon emission with absorption of a phonon, in which $E_p = k\theta$ is the phonon energy (after [4]).

The emitted spectrum intensity is the product of the indirect recombination probability [24] and the available free electrons in the conduction band and holes in the valance band that obey Maxwell distribution. The rate of emission is then:

$$R(h\nu) \sim \frac{32\pi^3}{c^3h^4} n^2 (h\nu)^2 \left[h\nu \frac{dn}{d(h\nu)} + n \right] \int_{E_v} \int_{E_c} \exp\left[-\frac{(E_c - E_v - \Delta F)}{kT} \right] \times (E_c - E_g)^{1/2} (-E_v)^{1/2} \times \delta(E_v - E_c + h\nu \pm k\theta) dE_c dE_v \quad (2)$$

in which

n - refractive index of silicon

T - lattice temperature

E_c, E_v - conduction band and valance band energy

$h\nu$, $k\theta$ - photon and phonon energy

E_g - the energy bandgap

$\Delta F = F_n - F_p$ difference of quasi-Fermi level of e and h

Reverse bias

It has been known since 1955 that a silicon p-n junction emits visible light under avalanche breakdown condition [3]. Yet the photon generation mechanism of this phenomenon is still not conclusive. Theories were proposed but failed to explain the variety of experimental results. Generally, this phenomenon is regarded as a field accelerated process and was explained in literature by a number of mechanisms that can be classified in to two main categories

- The interband (band to band) mechanism with direct and indirect recombination of conduction band electrons and valance band holes. The mechanisms in this category cannot produce photons with energy smaller than the energy band gap. The indirect process is commonly

assisted by phonons. The band to impurity level transition is considered to have much less probability [4].

- The intraband (single band) transition involves only one type of carrier electrons or holes within their respective energy band. The transition can be direct or indirect. The indirect process is assisted by phonon or impurity ions.

In the next subsections, consideration is taken on the mechanisms that are likely to contribute.

Indirect interband radiation under high field condition

This process considers [15] the recombination of electrons and holes occurring through a two-step process involving the interaction of an electron simultaneously with a hole and a phonon accompanied by the emission of a photon, similar to the forward bias emission mechanism, but with the presence of a local strong electrical field. Under that condition, the emission spectrum comprises of all the possible transitions between any pair of states separated by a given $h\nu$, regardless of the difference in crystal momentum between initial and final states. The emitted spectrum though has a theoretically low energy cut-off determined by $h\nu = E_g - E_p$, where E_p is the maximum energy of the emitted phonon assisting the transition.

$$I(\nu) \sim n^2 \left[\nu \frac{dn}{d(\nu)} + n \right] \nu^2 A \exp\left[-\frac{(h\nu + k\theta)}{kT} \right] \exp\left[\frac{(h\nu + k\theta)}{kT_h} \right] \exp\left[\frac{-aA}{2} \right] I_1\left(\frac{a}{2} \right) \tag{3}$$

in which,

$a = 1/kT_e + 1/kT_h$

$A = (h\nu + k\theta - Eg)$

$k\theta$ – phonon energy

I_1 – modified Bessel function of order 1

Bremsstrahlung radiation

This mechanism was considered first by Figielski and Torun in reference [6]. It is also called indirect intraband mechanism. The theory explains the visible light emission from silicon p-n junction by the deceleration effect of the Coulomb field of charged centers on hot electrons. The energy is conserved by the emission of a photon and the momentum is transferred to the

interactive positive core. If a Maxwell carrier distribution is assumed, the emission intensity can be calculated:

$$I(\nu) \sim C \exp\left(-\frac{h\nu}{kT_e}\right) \tag{4}$$

with T_e – the electron temperature. This is a monotonic response over the whole spectrum. This mechanism was widely accepted as one of the main mechanism for avalanche breakdown emission but recently it has been criticized in a few publications [7]. The criticism is based on the fact that electrons with energy of one eV or larger above the conduction band minima may not be estimated with effective mass theory because the parabolic approximation of the energy versus wave vector *E(k)* only works in the neighborhood of conduction band minimum. Moreover, the Maxwell distribution is erroneous at high field conditions.

Direct interband transitions

This mechanism involves the direct transition of energetic carriers with momentum *k~0* due to the fact that the threshold energy of e-h pair production by ionization is around 2.3 eV above the conduction band edge [9]. The population of hot electrons at this level is effectively depopulated leading to the high-energy cutoff in the spectrum around *Eg+2.3eV~3.4eV*. Energetic electrons around *k~0* may find corresponding states in the valence band for a direct recombination, constructing the high-energy part of the avalanche emission spectrum. This process was described using the following formula [9].

$$I(\nu) \sim B_1(h\nu - E_g)^{1/2} h\nu.[1 + B_2(h\nu / W)]\exp[-(h\nu / W)] \tag{5}$$

W - dependent on the electrical field and mean free path $W \sim kT$

B_2 - dependent on the exponential integral $\overline{E_i}$ of E_o / W

B_1 – empirically determined constant

E_o - the energy threshold for pair production

This equation provides a monotonic response over the whole visible range.

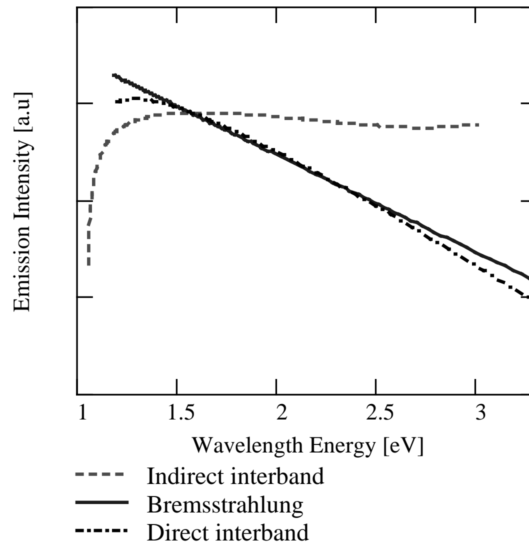

Figure III.1-2. Representation of calculated rate of emission of different mechanisms in reverse bias avalanche breakdown

The combination of these mechanisms into a multi-mechanism model has been published in [10] and that is employed to explain our results in the following section. A representative graph of the interested mechanisms is reproduced in Figure III.1-2.

III.2 Experiment

A schematic cross section of the devices we studied is depicted in Figure III.2-1. The fabrication process has been described in detail in chapter II. The antifuses have been created on 5μm× 5μm and 10μm × 10μm capacitors.

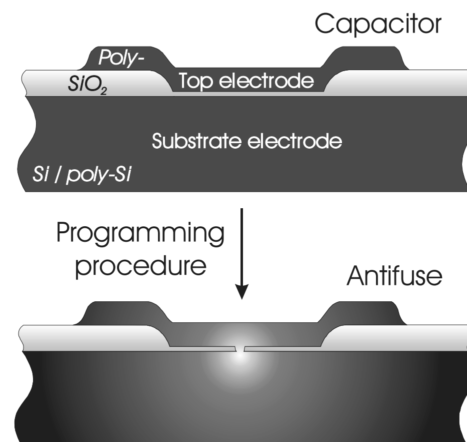

Figure III.2-1. Cross section of the studied structure; programming of the devices is done by forcing a limited current through the capacitor until breakdown occurs, resulting in the formation of a diode-antifuse

The experimental setup shown in Figure III.2-2 was used to record the photon emission spectrum of the diode-antifuses. As the light goes through the microscope, it is fed through a prism and focusing lens. After this the image of the spectrum is projected on a photo-cathode, amplified by a multi-channel plate and projected onto a phosphor screen in front of a CCD imager chip. The spectral range of the whole system is mainly determined by the photo-cathode material (S25) and restricted to the energy range of about 1.35 eV to 3.2 eV (900-390 nm). Output intensity $I(\lambda)$ is measured as the light power per unit wavelength, λ, in [W/nm]. This is later converted to $I(E)$, the light power per unit energy, E, in [W/eV], using the relation: $I(E) = 10^{-9}\frac{\lambda^2}{hc}I(\lambda)$, where λ is in [nm] and E is in [eV].

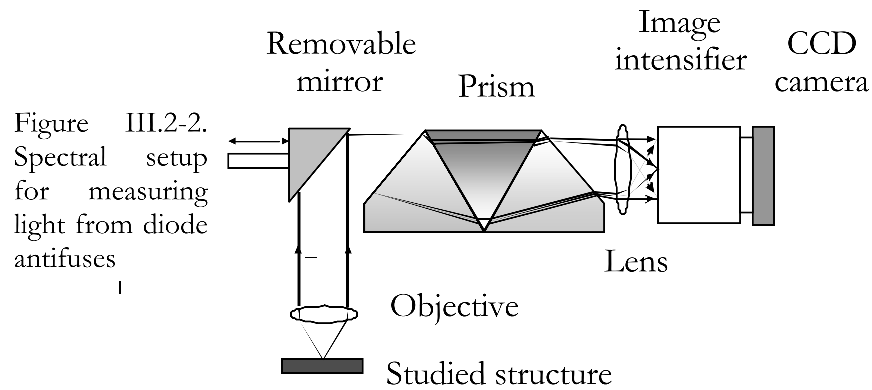

Figure III.2-2. Spectral setup for measuring light from diode antifuses

III.3 Results

Light emission measurements were performed on the diode-antifuses with highly doped substrate (HDS) and lightly doped substrate (LDS). The emission spectra of the HDS diode-antifuses measured at room temperature are shown in Figure III.3-1. (a and b) for various reverse and forward currents I_r and I_f, respectively. The integrated output power detected for the energy range of 1.4 – 3 eV is about 0.7 nW and 0.4 pW for 10 mA reverse and forward currents, respectively. In the case of LDS devices, emission spectra were measured only for different forward currents I_f, (Figure III.3-2). The output power detected for the energy range of 1.4 – 3 eV is 2 pW (at 10 mA). Reverse biased emission of LDS was not considered due to the very high breakdown voltage of these devices.

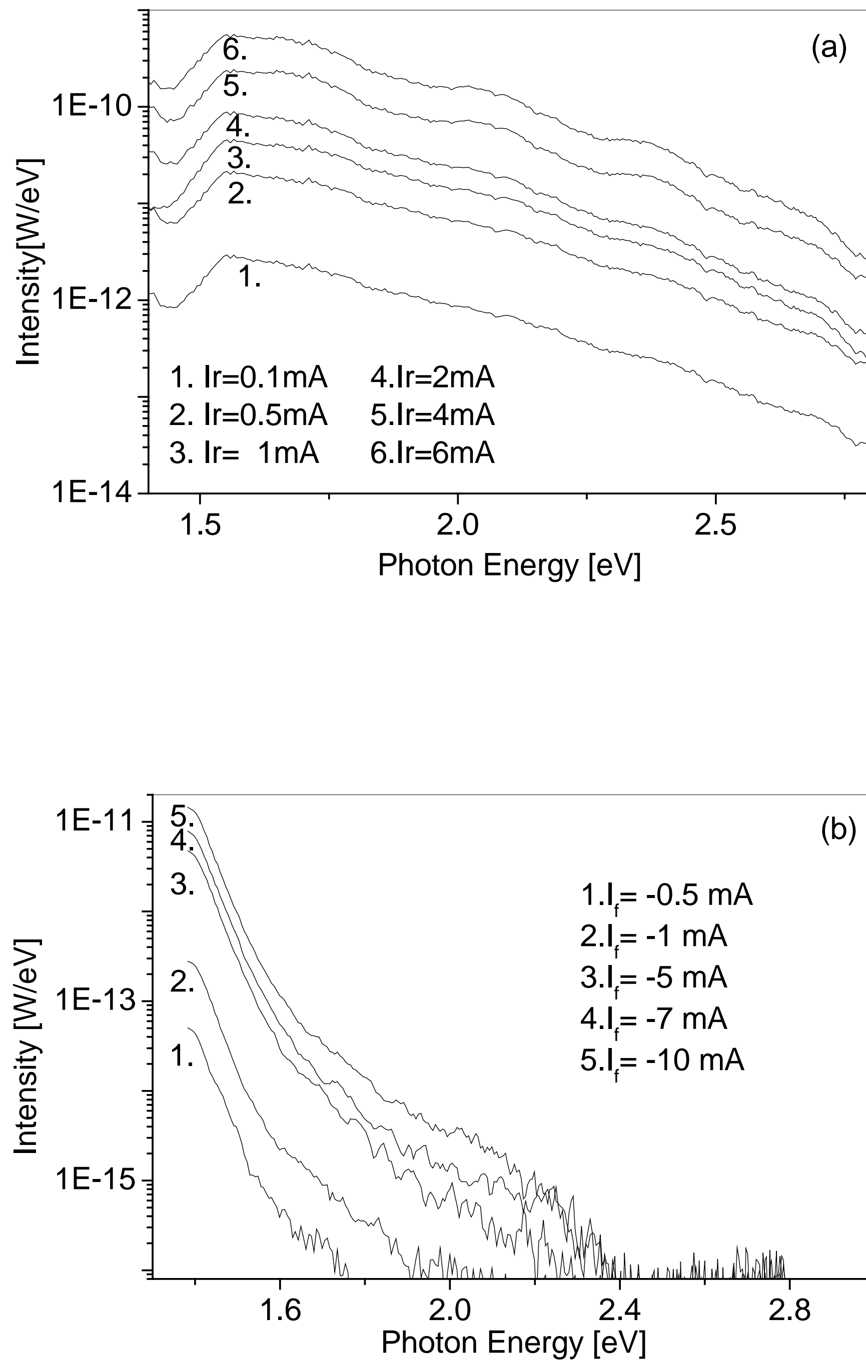

Figure III.3-1. Emission spectra of the diode-antifuse with highly doped substrate (HDS) measured at room temperature with (a) the diodes biased at different reverse currents I_r, (b) the diodes biased at different forward currents I_f.

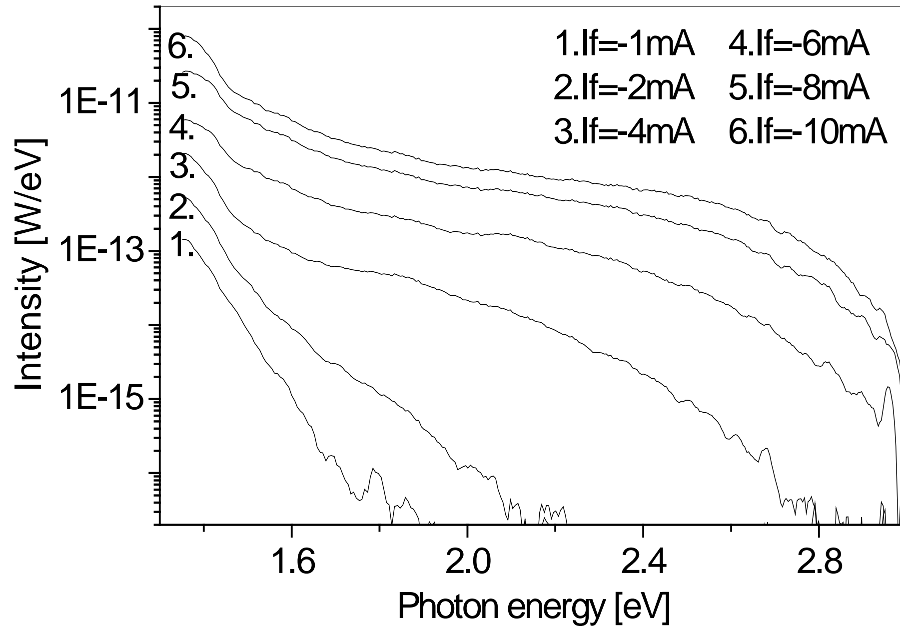

Figure III.3-2. Emission spectra of the diode-antifuse with lowly doped substrate (LDS) measured at room temperature with the antifuse biased at different forward currents I_f.

The emission spectra shown in Figure III.3-1(a) are similar to those reported from conventionally fabricated avalanche silicon p-n junctions [4][11]. A linear dependence between the integrated EL intensity and electrical input power is obtained (Figure III.4-6b). A distinguished difference in the spectral shape between the two cases of forward bias for HDS and LDS devices can be observed (Figure III.3-1.b and Figure III.3-2). In the former, the light is emitted mainly in the near infrared region, while in the latter case visible light is also strongly emitted in addition to the near infrared signal.

The origin of the light emitted in both reverse and forward modes will be discussed in the next section. The periodic patterns observed in the EL spectra are independent of the current and oxide thickness and are caused by the interference of the light reflected at the surface and the bottom of the n^+-polysilicon gate.

III.4 Discussion

III.4.1 Forward biased emission

Emission spectra from forward-biased HDS and LDS antifuses, at I_f= −10mA, are compared in Figure III.4-1. This current was achieved by applying a gate voltage of −5.5 V and −25.5 V for HDS and LDS respectively. The experimental values in Figure III.4-1 were normalized at the maximum intensity, showing an obvious difference between the two spectra. In the case of HDS devices, the emission is mainly in the near infrared region. Spectra measured from standard forward biased silicon junctions show also an emission in the near infrared region around the band gap of silicon [5]. The origin of this emission is attributed to the indirect interband recombination between electrons and holes. However, in the case of LDS devices, the light is emitted in a wide energy range, from the near infra-red far into the visible, with an intensity of about two orders of magnitude higher than that obtained from HDS at 2 eV. The visible part of the wide spectrum has never been observed in forward-biased silicon junctions.

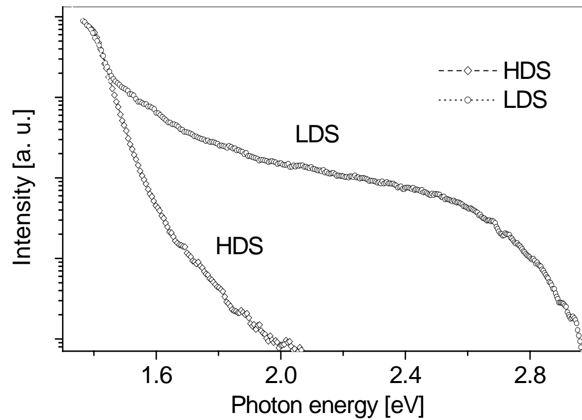

Figure III.4-1. Measured spectra from LDS and HDS diode-antifuse biased at forward current I_f = –10mA.

Infrared emission

For both LDS and HDS devices, the forward emission spectra show a maximum intensity below 1.35 eV (limit of the measurement system). It is understood that the mechanism responsible for this infrared emission is the phonon-assisted electron-hole recombination. Above 1.45 eV the measured intensity from HDS devices drop sharply, indicating that phonon-assisted

electron-hole recombination is the main mechanism responsible for the emission from the HDS devices. On the other hand, emitted intensity from LDS devices drops slowly towards high energies above 1.45 eV indicating that some other mechanisms are responsible for the visible light besides the phonon-assisted electron-hole recombination in the infrared. The visible light from LDS devices will be discussed next.

Visible emission

For LDS devices, because of the relatively high intensity of the spectra above 1.45 eV, a question arises whether the light is emitted from the forward biased junction or from another origin; hence the determination of the voltage across the oxide is needed. To force a forward current of −10mA, a voltage of −25.5 V was applied. In fact, the voltage on the gate, V_g, is applied across the series combination of the junction, the resistance of the conductive link R_{link}, all in parallel with the resistance of the oxide R_{FN} and finally the resistance of the p-substrate R_{sub}. An illustration of the equivalent circuit of the diode-antifuse is depicted in Figure III.4-2.

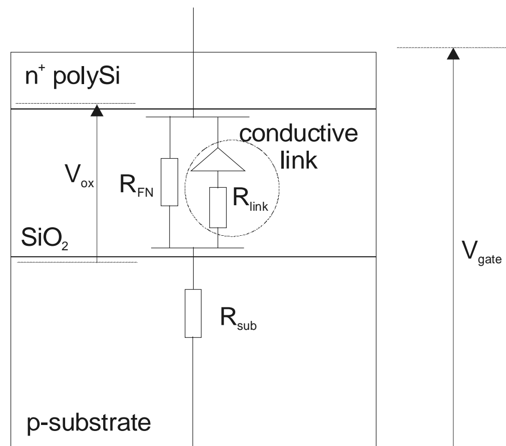

Figure III.4-2. Equivalent circuit of the diode-antifuse with the assumption that the resistance of the highly doped polysilicon layer is negligible.

The resistance of the poly-n^+ was neglected due to the high doping concentration. In the case of high level injection forward current, we can suppose that the series resistance of the device is R_s:

$$R_s = \frac{R_l \times R_{FN}}{R_l + R_{FN}} + R_{sub} \tag{6}$$

This value can be determined by the extraction of the series resistance from the linear part of the forward I-V characteristics of the diode-antifuse (Figure III.4-3). It was found that the series resistance is about 1.5 KΩ for LDS devices. For a current of I_f=–10mA, the voltage drop in the substrate is equal to $I_f \times R_{sub} > I_f \times R_s = -15V$. From this we can conclude that for a current I_f = –10mA the voltage applied to the oxide $V_{ox} = V_g - I_f \times R_{sub} < -25.5 + 15V$, meaning $|V_{ox}|$ > 10.5 V. The fact that $|V_{ox}|$ > 10.5 V indicates the electrical field applied to the 5.6 nm thin oxide is about 1.75×10^7 V/cm which is enough to allow electrons to tunnel into the oxide by Fowler-Nordheim (FN) tunneling (threshold for FN tunneling is about 5×10^6V/cm). Moreover, when the forward current is low, for example I_f = –1mA (corresponding to an applied gate voltage V_g = –5V), the emitted spectrum drops off in the near infrared region and no visible light is observed as shown in Figure III.3-2. This confirms that the visible emission is related to electron tunneling phenomena through the oxide outside the region of breakdown when the voltage is high. Similar calculations have been made for HDS devices with the value of the oxide electrical field about one order of magnitude lower compared to the LDS case. That is why visible emission is not observed in forward biased HDS diode-antifuses. In fact, several visible emission spectra have been reported in literature from tunnel current MOS devices [21][22], and different mechanisms of the emitted light have been discussed.

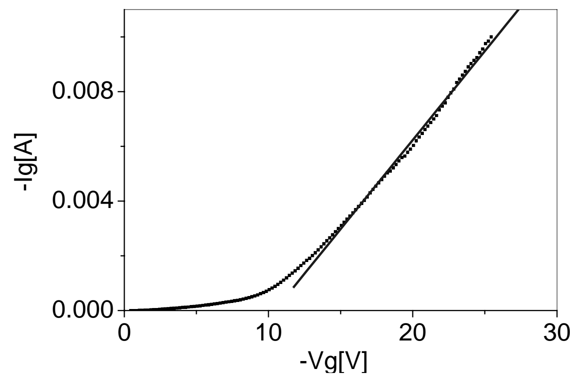

Figure III.4-3. Forward I-V characteristics of the LDS diode-antifuse showing the linear part due to the series resistance

Takagi et al. [23] found that electrons in stress-induced leakage current (SILC) are dominated by an inelastic tunneling mechanism accompanied by large energy loss of around 1.5 eV. Matsuda et al. [21] proposed that radiative electron capture into SiO_2 trap levels is responsible for emitted visible light from MOS capacitors with Si-implanted SiO_2. Qi et al [22] explain the visible electroluminescence observed from Au film/extra thin Si-rich silicon oxide film/p-Si by electron-hole pair recombination via several groups of luminescence centers in SiO_2 layers. They present this mechanism as responsible for the emission above 1.5 eV. As we discussed above, in the case of LDS devices, a part of the carriers is still tunneling through the SiO_2, and therefore recombination between electrons and holes via luminescent centers in the SiO_2 or electron capture into SiO_2 trap levels can occur. Besides, the tunneling electrons are injected into the conduction band of the Si-bulk with energies higher than 3.1 eV. These hot electrons may lose their energies by radiative recombination with holes in the accumulated p-Si surface or by transitions into the conduction band of the Si-substrate. The photons emitted by the former mechanism may have energies higher than 3.1+1.1= 4.2 eV, which could not contribute in our spectral measurement in the visible range. The latter mechanism is consistent with the experimental high-energy end around 3 eV.

In summary, it is very unlikely that the visible emission of LDS devices originates from the junction. It is more probable that the visible light has its origin from electron captured into SiO_2 trap levels and transition of hot injected electrons into the conduction band of the Si-bulk of diode antifuses.

III.4.2 Reversed biased emission

Figure III.3-1(a) shows that emission spectra measured from highly doped substrate diode-antifuses are similar to those reported from reverse-biased conventionally fabricated silicon p-n junctions. However, results that were reported in the literature are of a wide variety. Chynoweth and McKay [5] show a spectral intensity increasing over the infrared region. Newman's spectra [3] peak at about 2 eV; Haecker [8] reports intensity decreases below 0.8 eV. Gupta et al. [12] observe a maximum at 1.5 eV. Several attempts have been made to understand the origin of emitted light [13]–[17]. Previously published analytical or theoretical expressions do not fit the variety of results

reported in the literature, nor establish which mechanisms dominate under what conditions.

Recently, in reference [10] a multi-mechanism model for avalanche emission spectra from silicon junctions was proposed. This model indicates that indirect recombination of electrons and holes in high-field populations is the dominant emission mechanism at low photon energies, that indirect intraband transition dominates at intermediate energies, and that direct interband recombination between high-field populations of carriers near k~0 dominates above ~2.3 eV. Figure III.4-4 illustrates the above three mechanisms. Using this multi-mechanism model, differences between experimental spectra can be attributed to different values of electrical field strength and ionization length for electrons and holes in the variety of samples and structures used by researchers. Figure III.4-5 shows the multi-mechanism model described in [10] compared qualitatively to the measured spectrum of reverse-biased diode-antifuses.

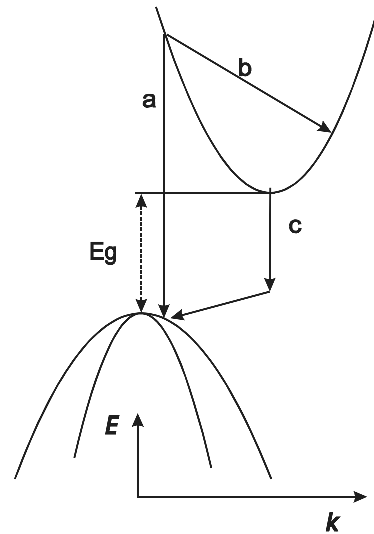

Figure III.4-4. Simplified silicon energy band; the arrows represent: a) direct interband recombination, b) intraband transitions (Bremsstrahlung), c) indirect interband recombination.

A silicon temperature of 280°C, electrical field of 3.3×10^5V/cm, electron temperature of 5000 K, ionization lengths for electrons and holes of 68 Å provide best fit to the maximum intensity observed in spectra at about 1.6 eV (Figure III.4-5).

T_{Si}	280°C
E field	3.3×10^5V/cm
l^e_{ioniz}, l^h_{ioniz}	68Å
T_e	5000K

Results of reference [10] indicate that the transition from indirect interband to Bremsstrahlung processes occurs at an energy that depends on applied

electric field; this transition shifts to lower energies at higher applied fields. The shift of transition point energy is consistent with field-induced rises in electron temperature, which enable higher energy Bremsstrahlung events. The transition from Bremsstrahlung to direct (and near direct) interband contributions is field invariant, with an energy position 2.3 eV. This value is the highest a photon can have from a Bremsstrahlung transition within the conduction band.

A multi-layer interference calculation has been incorporated to account for interference of the emitted light within the poly-Si layer [18][19]. The good agreement between the measured and the calculated spectra in Figure III.4-5 indicates that the light emission from reverse-biased diode-antifuses is caused by the same mechanisms as avalanche breakdown emission from standard p-n junctions.

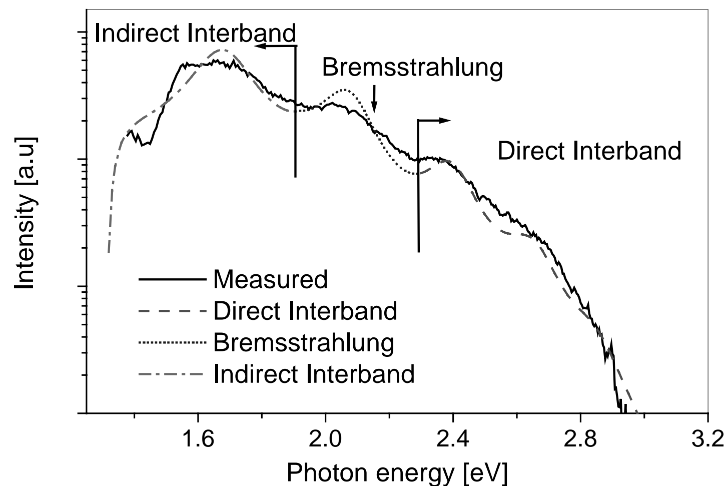

Figure III.4-5. Comparison of HDS diode-antifuse spectrum with the multi-mechanism model calculation result

It was found that the emitted intensity had a linear dependence on the current (Figure III.4-6). The reason for this linearity is elucidated in the following. During avalanche breakdown, the minority carriers are generated in the depletion region and accelerated by the high electrical field. These carriers (electrons or holes) are accelerated, and at some point able to create an electron-hole pair that might participate in the radiative recombination. The emitted intensity is equal to the number of photons emitted by electron-hole

pair recombination and should then depend on [n]+[p]. That leads to a linear dependence of intensity versus current. This is confirmed by a simulation of the optical output versus current from a p-i-n structure operated at avalanche breakdown made by reference [20]. With the assumption that the emission is due to radiative recombination of 100% of electron-hole pairs generated in the neutral regions, they found a linear dependence between the intensity and the current. That may clarify why we have a linear dependence of intensity versus current in avalanche breakdown condition.

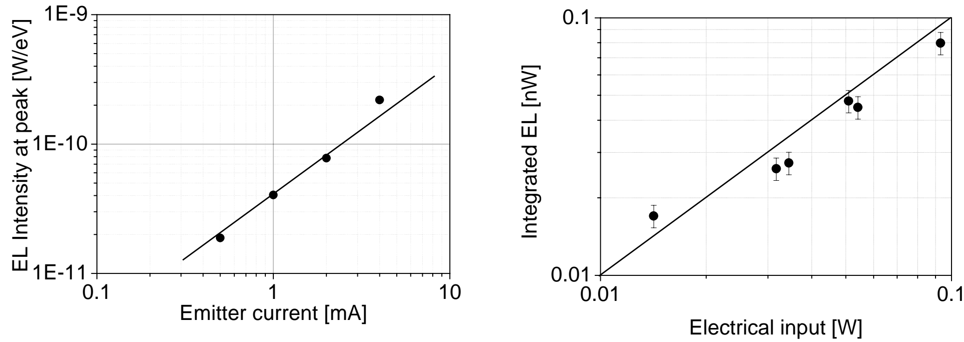

Figure III.4-6. Linear dependence of HDS maximum intensity versus current (a), Integrated EL versus electrical input power (b)

III.5 Conclusions

The electroluminescent properties of nanometer-scale silicon diode antifuses have been studied. The origin of the visible light emitted from reverse biased diode-antifuses was explained by a multi-mechanism model, which elucidates responsible processes for the light emission (indirect recombination of electrons and holes in high-field populations for low photon energies, indirect intraband transition for intermediate energies, and direct interband recombination between high-field populations of carriers near $k\sim0$ above ~2.3 eV). Diode-antifuses fabricated with lightly doped substrate (LDS) showed an emission in the infrared and the visible energy range when a forward current was applied at high gate bias. It was postulated that a phonon-assisted electron-hole recombination mechanism in the conductive link is responsible for the infrared emission. The visible light was attributed to current tunneling through SiO_2 (enabled presumably by electron capture into

SiO_2 trap levels) and to intraband transitions of hot electrons injected into the Si-bulk.

III.6 References

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Chapter IV

ANTIFUSE-BASED PHOTOCHEMISTRY

In this chapter, experiments using antifuses as an actuating element for implementing a microscale chemical process are described. Photons from the antifuse device illuminate a standard photoresist layer deposited on top of the emitting surface of the structure. The process of decomposition and/or polymerization in photoresist occurs as the device is switched on. The exposed resist is then developed in a standard developer solution. The features resulting from the process have been studied through other parameters such as the light emitting current, the exposure time… Based on the photoresist decomposition energy dose, the light emitting power of the antifuse in the near UV range could be approximately calculated. Due to the proximity between the layer and the light source, the power is interpreted on a more accurate basis. This research has also been proposed as a reliability detection method in modern integrated circuits.

IV.1 Introduction

The change induced in photoresist films when exposed to light is an example of photochemical detection of photons. Light produces a chemical change in photosensitive chemicals in the layer. The resist is then processed to convert the chemical change into an image. It depends on the processing method and materials whether the image is either positive or negative.

As discussed in the previous chapter, this research focuses on the so-called nanometer-scale diode antifuses, namely a deliberate link created between the two oppositely heavily doped (poly)-silicon electrodes of a thin oxide capacitor. The link behaves as a tiny p-n junction that emits visible and near UV light when biased in reverse breakdown mode. The advantages of diode-antifuses are IC-technology compatibility, very small size, multi-spectral light, and relatively higher efficiency… The drawback of the device is still the inherently low radiative recombination rate in silicon.

In this chapter, it is demonstrated how the photochemical reaction was carried out using this nanometer-scale lamp, and a simple application of the research to the field of IC reliability is tentatively proposed.

IV.2 Experiment

IV.2.1 Experimental details

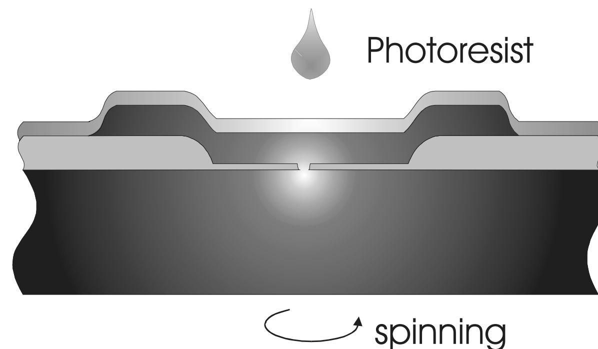

Figure IV.2-1. Test structure and resist deposition experiment

Wafers with simple antifuse devices were realized for these experiments. On top of the experimental devices, photoresist was deposited by dropping and spinning. When the device is operated under reverse biased breakdown

condition, i.e. the n-type doped electrode has positive bias, the upward emitted photons might be absorbed in the photoresist layer. The exposed resist chemically changes and become soluble in developer or insoluble when the image reversal technique is used.

A schematic cross section of the device is depicted in Figure IV.2-1. The respective thicknesses of the photoresist, which were developed either in a positive or negative way, are 0.85 μm and 0.5 μm and were measured by step height measurements with a DEKTAK surface profiler.

IV.2.2 Photolithographic image reversal technique [1]

Step 1: Standard positive resist process

Photo-active compound in resist (Dissolution Inhibitor) —UV / Exposure→ Dissolution Enhancer

Step 2: Reversal processing

Dissolution Enhancer —Reversal Bake / 90 –115 C→ Dissolution Inhibitor (Photo-inactive compound)

Dissolution Inhibitor (Photo-active compound, unexposed area) —Flood Exposure→ Dissolution Enhancer

Figure IV.2-2. Image reversal processing

The basic reaction of positive resist involves the conversion of the dissolution inhibitor to a dissolution enhancer. This dissolution enhancer can be thermally degraded and becomes an inhibitor again, which is however no longer photoactive. Under the proper conditions, this degradation can lead to the reversal of the resist image. The process can be described as in Figure IV.2-2. The process of using positive resist to obtain negative image is termed the image reversal or negative mode. The negative mode requires a reversal bake and a flood exposure. The flood exposure decomposes the unexposed resist to make them soluble in the developer and the area that was exposed in the first step remains insoluble. The difference of standard positive resist process and image reversal process is depicted in Figure IV.2-3.

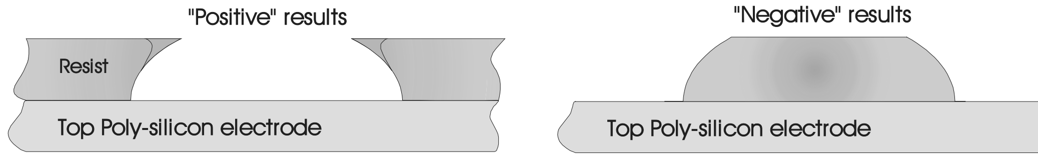

Figure IV.2-3. Final results of the two processes

IV.3 Results and Discussion

IV.3.1 Positive photoresist

Standard positive photoresist Oir 907/12 with a decomposition energy 110 mJ/cm^2) was used for this experiment. The meaning of "positive" is that the illuminated resist will be developed. This photoresist is specifically sensitive to photons with energy larger than 2.75 eV ($\lambda \leq 450$ nm). The exposed photoresist was developed using a standard developing process. A photographic picture of a feature is shown in Figure IV.3-1.

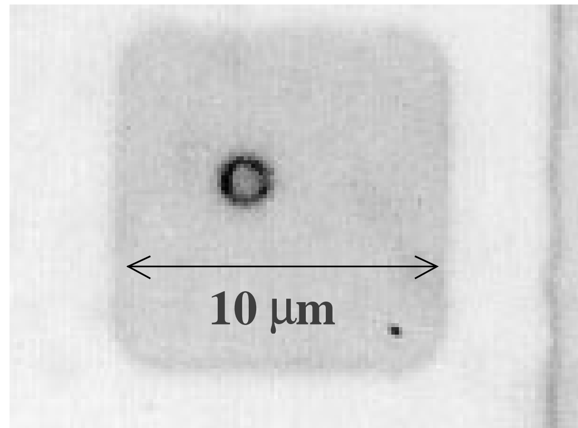

Figure IV.3-1. Feature developed in positive photoresist (I_r=1mA, t_{ex}=10min)

Photons emit upwards from the device but the developer is effective from the top resist surface, which implies that an adequate exposure time is needed to decompose the whole resist thickness up to the top surface of the resist, influencing the minimum feature size that can be obtained with positive resist. In Figure IV.3-2, some empirical points of the features' size are plotted against the time of exposure. The measured feature size is the averaged diameter of the inner light ring and the outer dark ring.

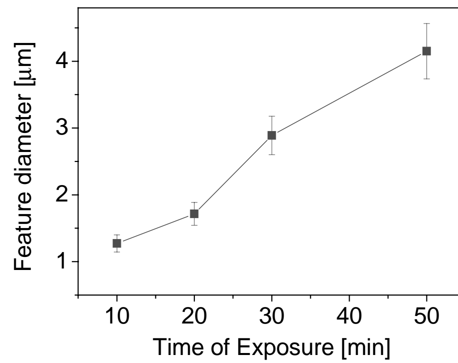

Figure IV.3-2. Average feature sizes versus exposure time at a constant exposure current I_r = 1 mA for positive photoresist

Near-UV light power

The antifuse light power in the near-UV was approximated, based on these values and the known decomposition energy. Given the photoresist decomposition energy dose of 110 mJ/cm2, a value of 3.4 pW photon power absorbed in the resist was obtained which means an external conversion power efficiency of roughly 7.10^{-10} of the near UV light power over the electrical input power of the antifuse.

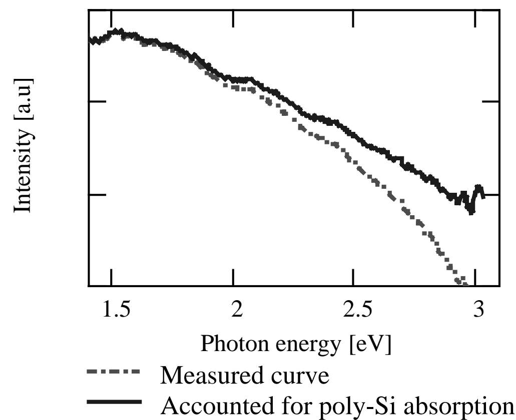

Figure IV.3-3. External light emission intensity as measured and corrected for internal absorption showing strong absorption in the near UV region by the poly-Si electrode

From basic laws of optics, it is clear that the UV-light illuminating the resist comes from a cone due to total reflection dictated by the relative refractive indices of silicon and resist, which is only a fraction of the spherically propagating light. Moreover, there is a considerable reflection at the poly-resist interface of light within this cone and strong UV light absorption in the top polysilicon electrode of the antifuse (see Figure IV.3-3). When the absorption is taken into account and the spherical emission is integrated the real internal UV light efficiency should be about two orders of magnitude higher.

IV.3.2 Image reversal

In order to obtain smaller size of the resist feature than that by the positive photoresist, a solution was implemented which employed the photolithographic image reversal technique, briefly described in section IV.2.2. Its advantage over the standard positive resist method is that very small features can be obtained (Figure IV.3-5, left) because the thickness of resist is not the limiting factor. The details of the developed resist feature are preserved for characterizations.

Scanning Electron Microscope (SEM) and Atomic Force Microscopy (AFM) were utilized to investigate the exposed resist dots. Comparisons were made on the accuracy of parameters obtained with each method. AFM measurements show a slightly larger diameter of the feature size than SEM. This is explained by the steep change of slopes at the base of the feature that exceed the reach of the AFM tip controller.

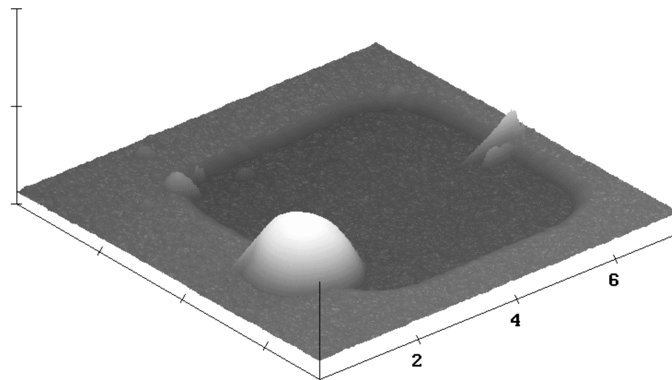

Figure IV.3-4. AFM image of an exposed photoresist dot

Experimental data were collected for building the relationships of size versus exposure current and exposure time respectively.

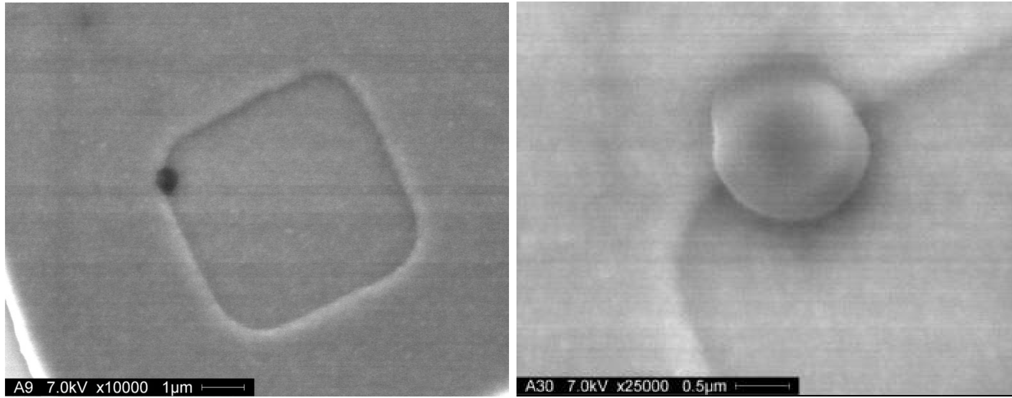

Figure IV.3-5. Developed features with image reversal technique: I_r=0.1mA, t=60min (left); I_r=3mA, t=20min (right)

Current dependence

A set of experimental data is shown in Figure IV.3-6. The data points were obtained by measurement of sizes of the large features with an optical microscope. Although it has been reported that instant light intensity and emitting current have a linear correlation [7][8], the feature size for an exposure current of 8mA is exceptionally large. This can be attributed to the influence of significant heat generation caused by the large current amplitude. Due to this side effect, the verification of more data is necessary in order to accomplish this dependency and the heating effect of the antifuse on the resist.

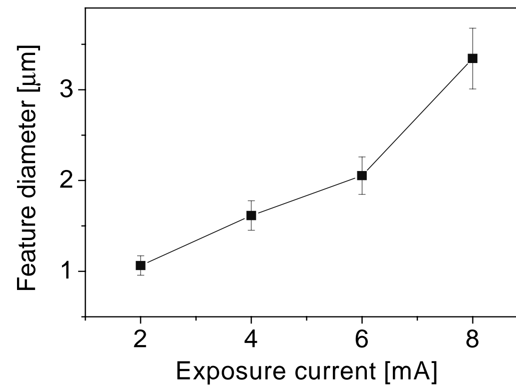

Figure IV.3-6. Average feature sizes versus exposure current at a constant exposure time t_r =5 min for positive photoresist

Exposure time dependence

For the time dependence, two sets of empirical data were obtained at two exposure currents of 0.1 mA and 3 mA. To determine a rough dependency by appropriate fitting between the two parameters, a simplified optical consideration has been investigated and presented below. The mathematical formulation fits well to the empirical results. The judgment on the physical meaning of coefficients reflects the appropriateness of the model.

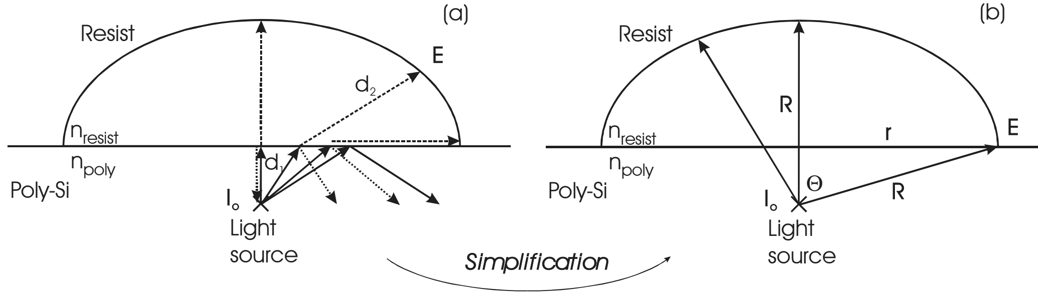

Figure IV.3-7. Classical optics consideration (a) and the simplification (b)

Let's assume that the light source is a point source and light is propagating equally in all directions and that a sharp interface between polysilicon and photoresist exists (no scattering at the interface). When a light wave travels to the interface, it undergoes a reflection and transmission process obeying fundamental laws of classical optics. The absorption process takes place both in the poly-Si electrode and the resist. The interference is neglected because the problem will be treated as an average, which is assumed to be eligible due to the large wavelength range considered and the thickness of polysilicon and resist being large compared to $\lambda/4n$. Furthermore, as has been seen in chapter III, the interference does not play a substantial role in the light emission spectra, which means it affects the light amplitude very slightly. Such arguments bring the problem to the situation sketched in Figure IV.3-7(a); any points on the resist feature surface will receive an equal amount of energy E that is derived as follows:

$$E \approx \frac{I_o}{(d_1 + d_2)^2} \exp(-\alpha_{poly}.d_1) \frac{4n_{resist} n_{poly}}{(n_{resist} + n_{poly})^2} \exp(-\alpha_{resist}.d_2) \tag{7}$$

with α_{poly}, α_{resist} - absorption coefficient of the polysilicon and the photoresist.

If the energy required to covert the resist chemically is T_o, then

$$T_o = E \times t \tag{8}$$

In which, t is the exposure time. Combining (1) and (2) and solving the equation will reveal the dependence of d_2 on t. However, this final equation is complicated and no explicit correlation between d_2 and t is possible. The simplification we consider is presented on Figure IV.3-7(b). Let's assume that $\alpha_{poly} \approx \alpha_{resist} = \alpha$ and $R \approx d_1 + d_2$. Point E on Figure IV.3-7(b) is in fact the measured position for the empirical diameter of the resist. As a result, the total energy received at point E for chemical conversion is:

$$T_o = E \times t = \left[\frac{I_o}{R^2} \exp(-\alpha R) \right] \times t = \left[\frac{I_o}{\sin^2\theta} \frac{1}{r^2} \exp(-\alpha \sin\theta \times r) \right] \times t \tag{9}$$

Taking $a = \frac{T_o \sin^2\theta}{I_o}$ and $b = \alpha \times \sin\theta$; then $t = ar^2 \exp(br)$. In a good approximation for $b \leq 1$ (b is the absorption coefficient) and r not too large (r is the feature radius), then $\exp(br) \approx \frac{1}{1 - br}$ leading to

$$t = ar^2 \frac{1}{1 - br} \tag{10}$$

The dependence of r on t is then

$$r(t) = \frac{1}{2a}\left[-bt + \sqrt{b^2t^2 + 4at} \right] \tag{11}$$

This equation has been used for fitting experimental data of feature size on exposure time Figure IV.3-8.

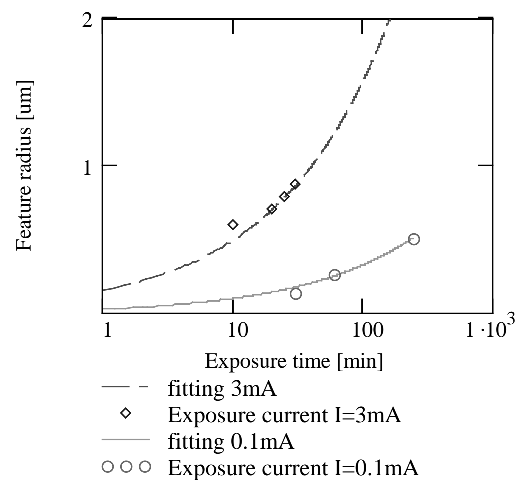

Figure IV.3-8. Fitting of the feature size on exposure time

This fitting law now can be used for predicting new exposure time dependence experiments.

IV.4 Proposal for a reliability detection method

A simple and inexpensive technique with high resolution to identify the weak spots in integrated circuits by means of a non-destructive photochemical process, in which photoresist is used as the photon detection tool, is proposed. Experiments were done to localize the breakdown position of thin silicon dioxide capacitors (the pre-devices of antifuses). Both positive and reversal development of photoresists were employed. The resultant products are holes in the developed positive photoresist layer and spots in the reversal case. The feature sizes, dependent on the light emitting currents and exposure time, establish an empirical correlation that can be used for further application of this technique as a reliability analysis tool. One potential application is to detect and characterize regions of hot carriers on a VLSI circuit under operation for design improvement purpose.

With further down scaling of VLSI integrated circuits (ICs), the high electrical field effects become a major problem. It is well known that under relevant conditions photons are emitted from nearly all silicon devices with hot carriers. For p-n junction diodes in avalanche breakdown, Newman already reported the light emission half a century ago [2]. The phenomenon is a consequence of the acceleration and multiplication of carriers by impact ionization in a high-field depletion region. Similar processes happen in bipolar transistors (BJT) and Junction Field Effect Transistors (JFET) if their collector/ base and drain/ gate junctions respectively are operated in reverse-bias conditions [2][3]. More seriously, the basic element of all present silicon ICs, i.e. sub-micron n-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET), also develops photon emission while operating in the saturation region [4]. These photons do not only influence neighboring devices but are also a source of power loss that should be prevented.

The oxide thickness of the MOSFET is another important parameter to be further scaled down in coming technology generations. The benefits are magnificent, especially capability to clock the chip at a much higher frequency. However, the unbalanced scaling down of the device sizes with the power supply voltage brings about the dielectric breakdown, namely, the failure of the thin silicon dioxide between the gate and the device channel [4]. At the location of this failure, there forms a link from the gate to the substrate especially in the case of hard breakdown. This link behaves as a nanoscale

junction diode, in case the gate and substrate have an oppositely doping type [4]. This failure mechanism is similar to the deliberate formation of the antifuse by fusing a capacitor (chapter II). The breakdown of thin dielectric layer becomes more severe in modern CMOS technology, as the gate silicon dioxide thicknesses reduce to few nanometers.

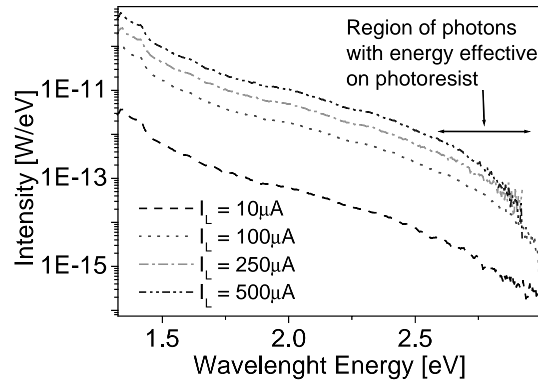

Figure IV.4-1. Recorded emission spectra of breakdown link at different currents

The emitted light spectrum has been recorded and explained elsewhere [6][7][8]. In general, it emits photons in the wavelength energy from around 1.1 eV to 3.3 eV, specifically, the visible and near ultra violet (UV) region. The measured spectrum presents a declining slope toward the high-energy wavelengths (Figure IV.4-1).

Photoresist, a UV light sensitive material, has been proposed as a detection tool. Image reversal technique demonstrates itself a suitable method with ease in handling and efficiency in resolution. The standard positive photoresist has drawbacks compared to the image reversal technique in the aspect of resolution and accuracy. CMOS standard photoresist types were employed to detect the spots of breakdown on 5×5 and 10×10 MOS capacitors. The capacitors have the same silicon dioxide thickness of 6nm. The technique has been successfully applied to determine the breakdown sites. Photoresist features as small as 300nm could be obtained so far. The resolution can probably be extended to less than 300nm with thinner photoresist layers and thinner poly-Si layers. This value suggests that this is a high-resolution non-electrical identification technique in comparison to other methods such as

liquid crystal (LC), infrared thermography (IR-T), which have a limited resolution of the order of a few μm [9][10].

IV.5 Conclusions

It has been shown that the diode antifuses induce photochemical reactions in photoresist. This fact indicates that microscale photon induced chemical processes are a feasible application of antifuse light sources. The resist has been proposed as a detection tool for defect localization and identification. The experimental results have been explained by a theoretical formulation, although a better quantitative model and analysis is still preferred.

IV.6 References

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Chapter V

INTEGRATED SILICON OPTO-ISOLATOR

The realization of a silicon electro-optical device based on monolithic CMOS integration of a silicon nanometer-scale diode antifuse with photodetector is reported. The light emitting diode antifuse operates in reverse biased breakdown condition (V_{BD}=3.5V). The photodetector windows are comparatively large to collect more the downward emitted photons. The overall electrical efficiency of the system is 1.10^{-6}, which is significantly larger than previously reported values. The improvement is attributed to the higher efficiency of the antifuse, and the collection of more photons on the detector owing to the straightforward coupling. This device demonstrates its feasibility as an optical sensor.

V.1 Introduction

With the progress of ULSI technology, the microelectronic devices have reached deep sub-micron features. However, signal propagation delay and latency in multi-level metal interconnections increase with decreasing feature size due to wiring resistance and capacitance. On-chip optoelectronic interconnections are investigated as a candidate for replacement with advantages such as fast speed, immunity against electromagnetic interference, reduced chip size…

The integration of light emitters, detectors and optical fibers on a silicon substrate is an important subject and receives great interest because it allows on-chip interconnects. Besides, such integration can create in the monolithic form an entire class of optical sensors that is currently realized by hybrid component integration and conventional packaging techniques, e.g. the hybrid approach of integrating GaAs emitters on silicon by wafer bonding was investigated in [1]. On the aspect of optical interconnects, the foremost obstacle is the integration of efficient and fast light emitters on silicon wafers through an IC technology compatible process. Recent advances in light emitting silicon devices (chapter I) have raised new expectations. In contrast, for realizing a monolithic optical sensor the high efficiency of the light source is not of the supreme importance compared to stability and reproducibility, which are now the prevailing concerns.

An IC compatible optical system, reported in reference [2], showed the first monolithic integration of light emitting diodes, detectors and optical fibers on a silicon wafer. The light emitter is a p-n junction operated in avalanche breakdown, the detector is another junction diode fabricated by ion implantation. The emitted photons are guided to the detector by a stoichiometric silicon nitride (Si_3N_4) waveguide with different lengths. The author claimed 30% optical coupling efficiency by a curvature arrangement at both ends of the fiber. However, the overall electrical efficiency is of only 6×10^{-8}. Experiments on the detection of patterned photoresist and binding of bio-molecules were done to show attenuation or increase of signal magnitude on the photodetector. The weakness of this structure lies at the separation of the emitter from the detector. The two devices were on the same wafer that jeopardizes the distinguishing of signal sources[3].

In [4], high-frequency silicon CMOS light emitting device with electro-optical interface was presented. The emitter realized utilizing a standard 2-μm industrial CMOS technology and processing procedure. The device and its associated driving circuitry were integrated in a CMOS circuit and capable of interfacing with a multimode optical fiber. The device emits light by means of a surface assisted Zener breakdown process that occurs laterally between concentrically arranged highly doped n^+ rings and a p^+ centroid, which are all co-planarly arranged with an optically transparent Si-SiO_2 interface. Calculation by the author showed 200MHz modulation capability. Unfortunately, the monolithic integration has not yet been demonstrated. The device may find applications in the sensor and actuator field.

In this chapter, the IC-compatible realization of a novel silicon electro-optical device is presented, explicitly the integration of nanometer-scale light emitting diode-antifuse and photodetector, or an opto-isolator. One of the advantages of this device is the complete separation between the emitter and the detector. Another is the emitter locates right above the detector providing a better coupling to the detector, which also means that the device is without a true light waveguide. The ratio of the generated photocurrent over the excitation current, technically called overall electrical efficiency, is over an order of magnitude larger than the value reported in [2]. The integration allows us to do different measurements on both forward- and reverse-biased emission from the nanometer-scale antifuses.

The following sections will discuss the device fabrication details, the different characteristics of the device, and optical consideration. An enhanced version of this device with an integrated channel sandwiched between the light source and the photodetector has been realized and will be discussed in the next chapter of this thesis.

V.2 Device Fabrication & Measurement

The device fabrication employed a six-mask IC compatible process (Figure V.2-1). First of all, photodetector windows were made on n-type silicon by implantation of boron. A layer of 100nm oxide was then deposited to electrically isolate the photodiode from the subsequent layers. Next, 10×10 μm^2 capacitors, with two oppositely doped poly-Si electrodes and a 8 nm thick LPCVD oxide, were deposited on top of the detector window.

Electrical contacts were finally made to the detector and the electrodes of the capacitor by aluminum sputtering and patterning.

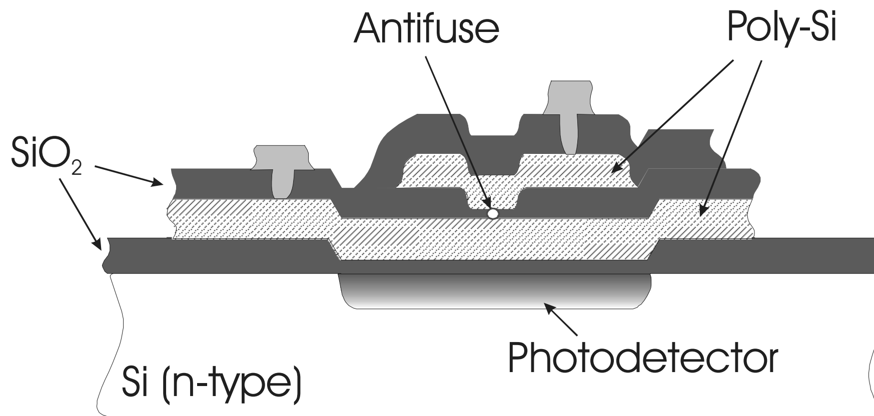

Figure V.2-1. Schematic illustration of the opto-isolator device

V.2.1 Working principle

The antifuse is created by controlled oxide breakdown between the two oppositely doped polysilicon electrodes. The antifuse emits light under electrical reverse biased breakdown. The photodetector window was large to collect the photons within the transmitted light cone defined by the total internal reflection law at the poly-Si and isolation oxide interface.

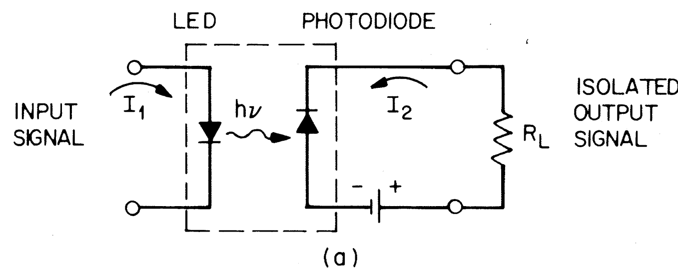

Figure V.2-2. Equivalent circuit of the device (After [8])

The LED current I_1, later called emitter current, is applied in reverse bias at different values. The photodiode current, further called detector current I_2, is measured by sweeping a voltage from forward to reverse bias on the two electrodes of the detector. Since the dark current is extremely small, the

current through the detector in reverse bias is the generated photocurrent induced by the absorbed photons (Figure V.2-1).

V.3 Results and discussion

The biggest obstacle that hinders the development of integrated optoelectronics on silicon is the integration of an efficient light emitter. The conventional avalanche breakdown light emission quantum efficiency is about 7×10^{-9} [4] to 6.5×10^{-8}[6]. These low figures were not only due to the light emitting mechanism, but also the loss of carriers to non-radiative recombination to the large planar area of the junction (most reports showed only light emission at the junction edge where the electrical field is higher). The nanometer-scale size of diode-antifuse light emitter solves those problems.

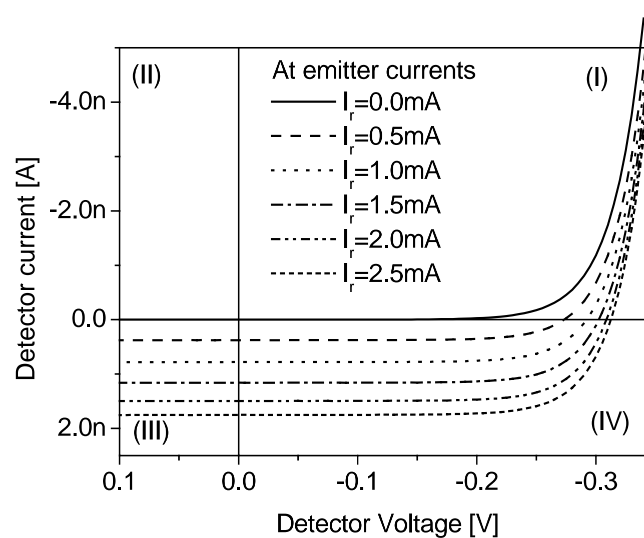

Figure V.3-1. Measured currents passing the photodetector at different emitter currents

In Figure V.3-1, the photocurrents of the detector are shown at different emitter currents of the antifuse. The graph shows the standard photodiode response with photocurrents increased corresponding to elevated emitter currents in the third and fourth quarter of the coordinate. It is clear from the graph that the device is truly an integrated opto-isolator. The precise efficiency of this system requires detailed calculation of light absorption and values of quantum efficiency of both the emitter and the detector.

V.3.1 Electrical characteristics

After the oxide has been charged till breakdown, programming currents up to 8 mA were applied to form high quality antifuses. The current voltage characteristics of the emitter and the detector are respectively represented on Figure V.3-2 (a) and (b). Figure V.3-2(a) indicates the on-set of breakdown voltage at approximately 3.5 V and an avalanche current of 1 mA at 8 V. The calculated series resistance based on the forward characteristics is approximately 4 kΩ. It comes largely from the spreading resistance of the antifuse (point contact) and from the thin film nature of both poly-Si electrodes.

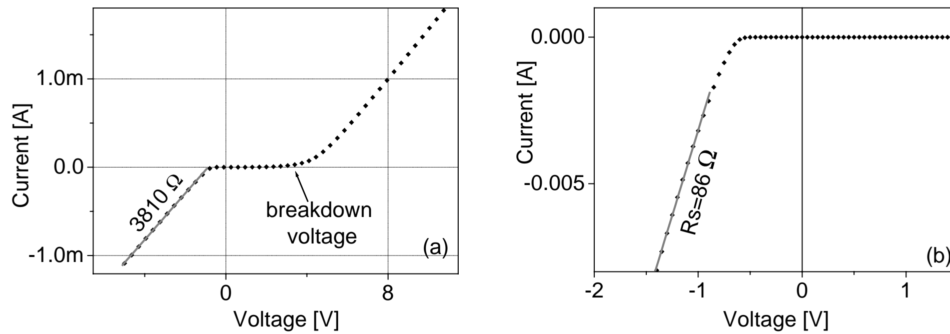

Figure V.3-2. Current voltage characteristic of light emitting diode antifuse (a) and photodetector (b)

The dark I-V characteristic of the photodetector is clearly a standard junction diode with low reverse current and small series resistance. The value of the resistance is rather high due to the non-optimal backside contact.

V.3.2 Overall electrical efficiency

A direct indication of the efficiency of the system is the ratio between the emitter current and detector current. This quotient is defined as the overall electrical efficiency, which is roughly 1×10^{-6} for this system. This value is about one order of magnitude larger than the one reported in reference [2], and simultaneously implies a higher external quantum efficiency of the antifuse compared to conventional diode [4][6].

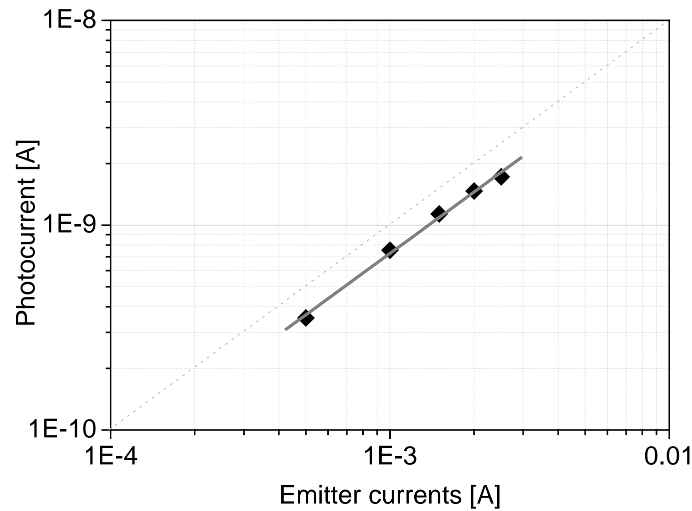

Figure V.3-3. Linear dependence between photodetector currents and antifuse light emitting currents

As seen in Figure V.3-3, the photocurrent has a linear correlation with the emitter current, which is a standard relationship of photodiode versus radiant flux of light incident on the device. The correlation could be inferred from the linear relationship between the integrated EL intensity against emitter electrical power in chapter III.

In reference [1] the overall electrical efficiency of a hybrid interconnection is 5×10^{-4}. The value reported in reference [2] is 6×10^{-8} for an all silicon system. Therefore, this device structure has progressed considerably towards the efficiency range of a hybrid system that employs efficient compound LEDs.

V.3.3 Evaluation of antifuse Power Conversion Efficiency (PCE)

With moderate simplification, the power conversion efficiency of the antifuse can be calculated from Figure V.3-3. The dissipated electrical power on the diode antifuse is easily measured. The optical power received on the detector can be converted to the radiance within the cone of light coming to the detector. The total flux then can be integrated over the sphere corresponding to a solid angle of 4π steradian. Due to the dependence of refractive index of silicon on wavelength, the solid angle $d\Omega$ of the cone is wavelength dependent for that same reason.

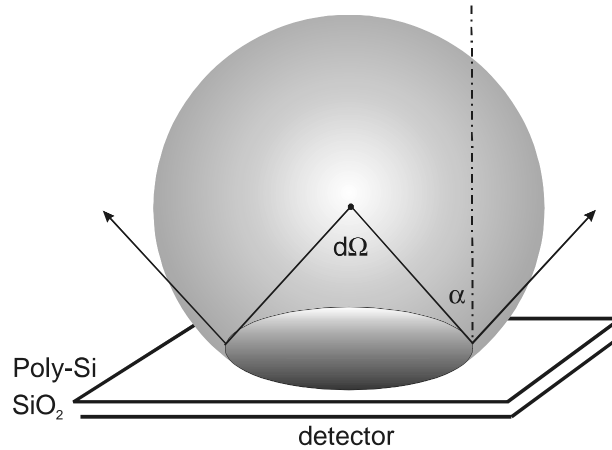

Figure V.3-4. Approximation for the PCE calculation

Let's assume a point source, monochromatic waves propagating spherically, and a cone of light with solid angle $d\Omega$. This angle is derived from the difference of refractive indices between polysilicon and silicon dioxide for this specific wavelenght. If the critical angle for total internal reflection at this poly-Si/SiO_2 interface is α, then $d\Omega$ is $\frac{\pi \sin^2(\alpha)}{\cos\alpha}$ steradian. If the power received within this solid angle at the detector is P, the power of the point source is P_o, the quotient of P over P_o is calculated as $\frac{P}{P_o} = \frac{d\Omega}{4\pi} = \frac{\sin^2(\alpha)}{4\cos\alpha}$, thus $P_o = \frac{4\cos\alpha}{\sin^2(\alpha)} P$. If α=0.4 radian (for λ=660nm), the measured optical power on the detector is P=0.3nW, the total emitted power by the source is then P_o =7.3nW. This means that the power conversion efficiency is also roughly 1.10^{-6}, as the electrical power is around 8mW (1mA, 8V). This estimation did not take into account that good silicon photodiodes have a conversion efficiency of 10÷25%, the reflection at the poly-Si/SiO_2 & SiO2/Si interfaces, and the absorption within the poly-Si layer, therefore the internal PCE of the antifuse is 10÷100 times higher.

V.3.4 Detection capability

The photocurrent is the indication of the amount of incident photons onto the detector. If the amount of photons can be regulated, for instance by means of a change of index of refraction on the top surface, the photocurrent

changes accordingly, which implies the detection capability of the photodetector. Experiments were implemented where air was replaced with a layer of silver paint. Due to this change in medium, there is a noticeable increase of the photocurrents as shown here in Figure V.3-5. This is possibly caused by the more reflection of photons back to the detector from the interface with the new material other than air. In the next paragraph a more quantitative analysis is presented.

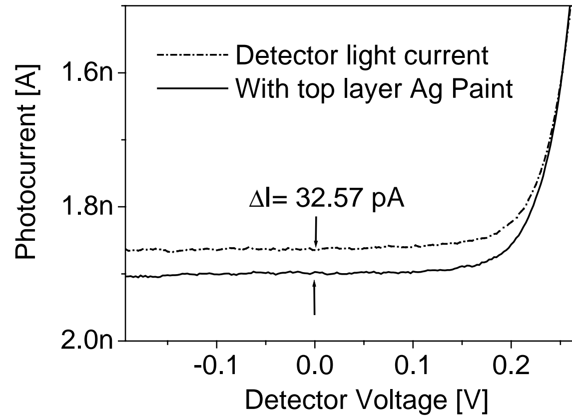

Figure V.3-5. Increased photodetector current due to a layer of silver paint on top of the device

Optical consideration

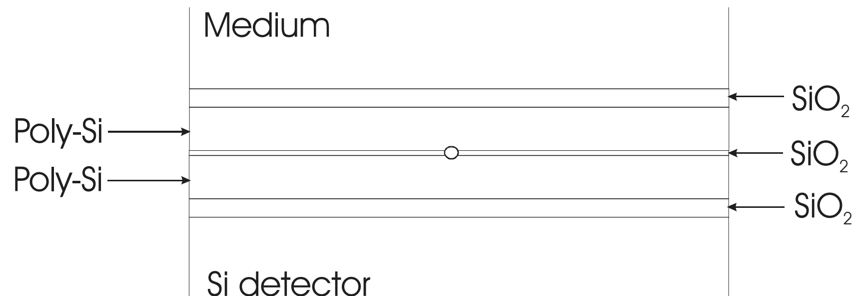

Figure V.3-6. Layers of the structure

In order to optically understand the detected signal, a reflection case for thin films has been considered. The structure consists of five layers, the top oxide layer beneath the open medium, the first polysilicon electrode, a thin antifuse oxide, the second polysilicon and the isolation oxide (Figure V.3-6) above the

silicon detector. The bottom medium is crystalline silicon where light is converted into electrical signals by the junction diode.

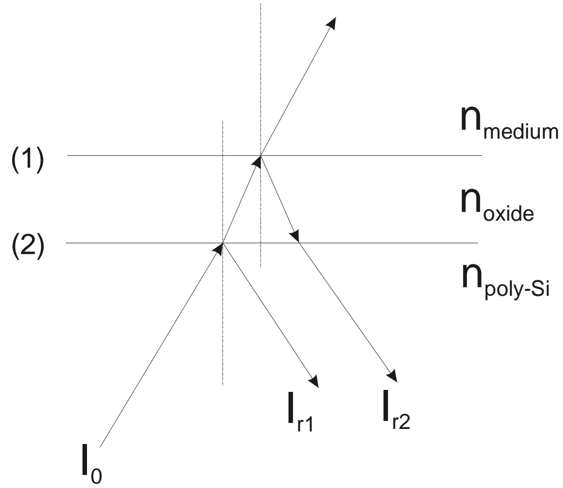

Figure V.3-7. The reflected waves at the oxide/medium interface back to the detector I_2 (absorption is not taken into account).

The simplified sketch in Figure V.3-7 can explain the reflection toward the detector at the top interface, where the medium and the two top layers are represented. Any lightwaves from the antifuse that come to the top oxide/medium interface at appropriate angles undergo reflection and refraction. The reflection portion will carry the information from that interface to the detector, in case it reaches this bottom medium. The situation at the front interfaces becomes a reflection from two parallel surfaces separated by a distance. At the first interface, the coefficients of amplitude transmission and reflectance are σ_1 and ρ_1, respectively, and at the second interface, they are σ_1 and ρ_1, respectively.

$$-\rho_1 = \frac{n_{poly-Si} - n_{oxide}}{n_{poly-Si} + n_{oxide}} \quad \rho_2 = \frac{n_{oxide} - n_{medium}}{n_{oxide} + n_{medium}} \tag{12}$$

The standard solution to this problem has been given in [7]. The reflection coefficient R is:

$$R = \frac{\rho_1^2 + \rho_2^2 - 2\rho_1\rho_2\cos\delta}{1 + \rho_1^2\rho_2^2 - 2\rho_1\rho_2\cos\delta} \tag{13}$$

in which, δ is the phase difference introduced by two consecutive reflections inside the middle layer $\delta = \left(\frac{2\pi n_{oxide}}{\lambda}\right)2t\cos\theta$.

If there is a change in the top interface, the reflection of light at the oxide/medium interface will be imaged by a change in value of ρ_2 and thus a different value of *R*. That change in reflection coefficient *R* is the reason for the detected signal on the photodetector shown on Figure V.3-5. In Figure V.3-8, a dependence of *R* on the wavelength is calculated for the medium refractive index of silver metal, oxide layer thickness of 100nm. The *x*-axis wavelength ranges from 400 nm till 1100 nm. The high average value of *R* in Figure V.3-8 puts the small signal increase in Figure V.3-5 in doubt. However, it can be explained by the fact that the reflected light will have to travel through a stack of 5 layers (Figure V.3-6), which absorbs a large portion of high energy photons before they could reach the detector. The photons which meet the total internal reflection would stay inside the stack and do not contribute to the current increase. Furthermore, those photons that actually reach the detector are those with long wavelengths, which may not be absorbed in the active region of the photodetector, due to the low spectral response of silicon for these wavelengths and thus do not contribute to the signal increase either.

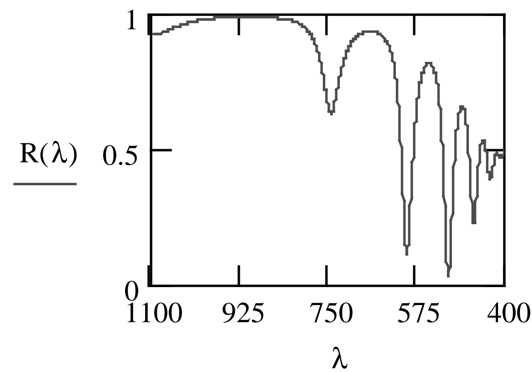

Figure V.3-8. Dependence of R on the wavelength λ

V.3.5 Stability

The system test of over 48 hours at constant emitting voltage results in a stable characteristics (Figure V.3-9). There is, however, a decay of detector current of about 20pA. The reason for this decay probably originated from the deviation of the emitter current. As discussed in chapter II, the emitter is created from the dielectric breakdown of the thin silicon dioxide capacitor, and stabilized by a large magnitude constant current. The increase of the emitter current over time observed in Figure V.3-9 is attributed to the degradation of the thin LPCVD deposited oxide layer. It is easily understood from the fact that this thin oxide layer did not receive adequate annealing procedure during the device fabrication process. An optimized process is

therefore required to improve the stability of the fuse oxide layer in particular and the system in general.

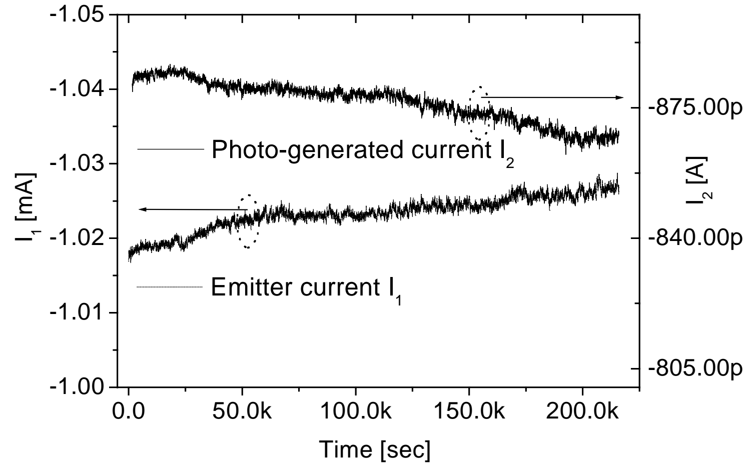

Figure V.3-9. Correlation between the emitter current I_1 (biased at 8V) and detector current I_2 over time; the detector is biased in photodiode regime and thus the photocurrent I_2 is measured

V.3.6 Antifuse in forward bias

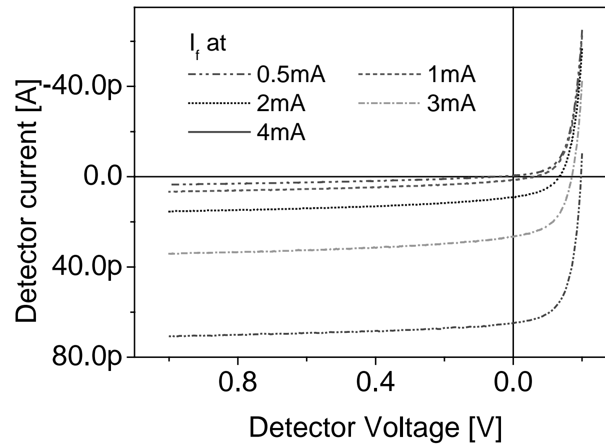

Figure V.3-10. Detector currents at different forward emitter currents

In forward biased mode of operation, it is known that HDS antifuses emit faint infrared photons (chapter III) around silicon bandgap. Making use of this integrated device, such weekly absorbed and small signals can still be detected as shown here in Figure V.3-10.

V.4 Conclusions

A monolithic electro-optical device has been demonstrated. The device is based on a light emitting diode antifuse and photodetector integrated on a single chip of IC compatible technology. The efficiency of the realized system indicates an important improvement for the realization of silicon optoelectronic devices. The signal generated by the refractive index change at the top surface of the device is detectable. The device is a demonstration of integrated optoelectronics on silicon.

V.5 References

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Chapter VI

NOVEL INTEGRATION OF MICROCHANNEL WITH SILICON LIGHT EMITTING DIODE-ANTIFUSE

Light emitting diode antifuses have been integrated into a microfluidic device that is realized with extended standard IC compatible technological steps. The device comprises of a microchannel sandwiched between a photodiode detector and a nanometer-scale diode antifuse light emitter. In this chapter, the device fabrication process, working principle and properties, and possible applications will be discussed. Changes in the interference fringe of the antifuse spectra due to the filling of the channel have been measured. Potential applications are electro-osmotic flow speed measurement, detection of absorptivity of liquids in the channel, detection of changes of the refractive index of the medium in the channel, e.g. air bubbles, particles in the liquid.

VI.1 Introduction

Silicon is well known as an electronic and mechanical material but it is hardly ever used as an active optoelectronic element, due to its inefficient radiative recombination over an indirect bandgap. Integrated silicon optical sensors themselves encounter that critical obstacle. Recently, silicon nanometer-scale diode antifuses have emerged as a reasonable choice with improved efficiency, small size, and IC-compatible fabrication[1][2], [chapter II & III]. In this chapter, it is proposed for the realization of a microfluidic device.

With the rapid growth of microfluidics and microchemical systems in research as well as in applications, specialized devices for sensing and measuring parameters are becoming increasingly important [6][7]. The integration of the light emitter and detector with a microscale fluid channel provides a universal tool for that purpose. This device structure also has possible applications in micro Total Analysis Systems (μTAS), (bio-)chemical sensors and actuators[4][5]. Furthermore, the approach can also give rise to new types of sensors.

The technology used in the creation of this device is a combination of standard CMOS technology with silicon micromachining technology. The antifuse and photodiode were realized with standard CMOS steps, but the microchannel required a sacrificial poly-Si etch in potassium hydroxide (KOH). However, a fully CMOS compatible etching recipe using Tetra Methyl Ammonium Hydroxide (TMAH) might be an option (discussed in VI.4).

In the next sections of this chapter, the fabrication process, some critical technological design parameters, electrical and optical properties, and a few results will be described respectively.

VI.2 Device realization

The realization of the device (Figure VI.2-1) requires a 10-mask process. The starting material is a 3-inch silicon n-type phosphorus doped wafer with resistivity of 5-20 Ωcm^{-1}. Firstly, the junction photodiode areas were fabricated by implantation of boron. To prevent any step height difference at the junction between the n-type and p-type region, thick resist was used as

masking layer for the implantation. This is important to the evenness of the channel.

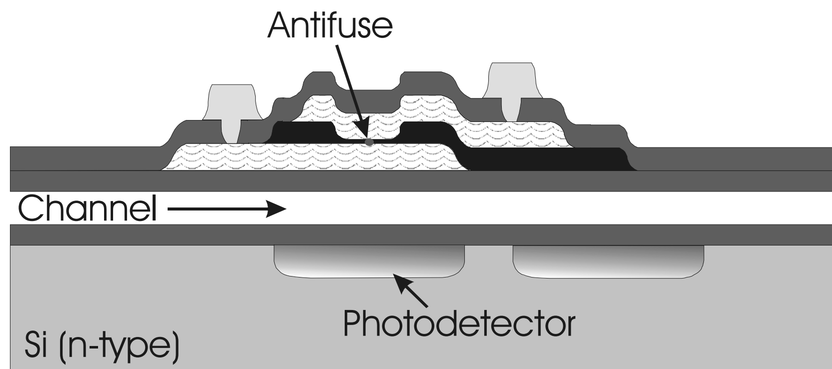

Figure VI.2-1. Schematic drawing of the integrated device

Layer	*Thickness*
1st, 2nd, 3rd SiRN	500 nm
1st, 2nd Poly-Si electrodes	300 nm
Channel W×L×H	10μm×2000μm×0.5μm
Antifuse dielectric layer	8nm

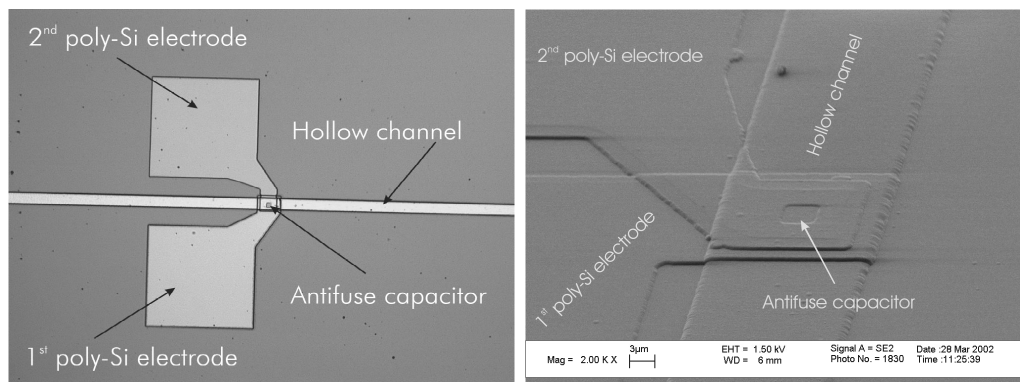

Figure VI.2-2. Channel under the antifuse window, two polysilicon electrodes of the antifuse capacitor structure are clearly visible

The shape of channels were then produced by shaping a layer of 500 nm thick LPCVD polysilicon deposited on top of the first silicon-rich nitride (SiRN) layer. Next another SiRN film is deposited to completely cover the

polysilicon. These two SiRN layers act respectively as the top, bottom and sidewalls of the channel opened later by sacrificial polysilicon etching in KOH. They also electrically isolate the detector and integrated antifuse from the channel.

On top of the second SiRN layer, a capacitor structure with size of 5×5 μm^2 is fabricated. The first electrode is 300 nm phosphorus implanted polysilicon. The capacitor dielectric layer is 8 nm LPCVD deposited silicon dioxide. The second polysilicon electrode was implanted with BF_2 with a dose of $3.10^{15} cm^{-2}$ at 70 keV (Figure VI.2-2). The activation of all dopants were simultaneously done in the next step while a protection layer of SiRN was deposited at 850°C for approximately 90 min. Next, for the opening of the channel, windows at two channel ends were patterned and etched until reaching the sacrificial polysilicon. The 25 wt%, 75°C KOH etches polysilicon at a rate of roughly 1 μm per minute. That means a channel of 2 mm would take nearly 1.5 days of etching [3]. However, the silicon wafer is well protected because of the negligible etching of SiRN in KOH solution. SiRN was also chosen for the process due to its low mechanical stress compared to stoichiometric silicon nitride. As the channel etched through, the processed wafer then needed a standard treatment to dissolve alkali ions and other contaminations.

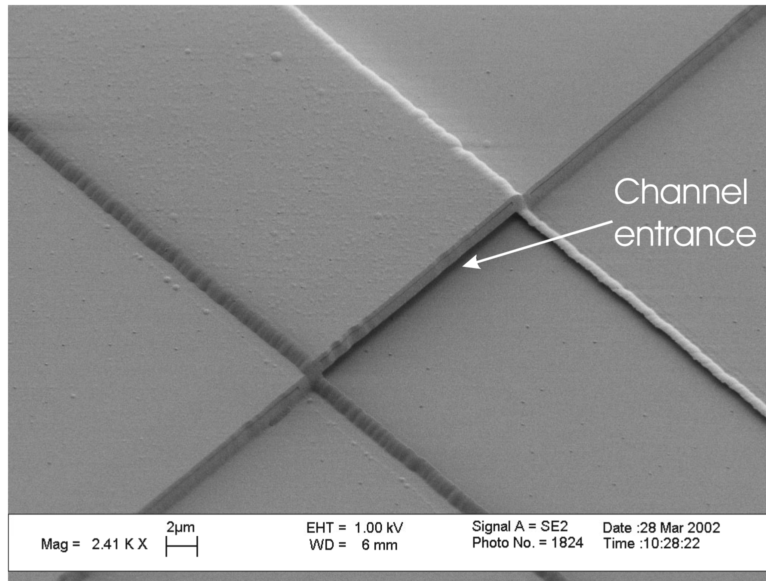

Figure VI.2-3. SEM image of channel entrance

The inner surfaces of the channel needed a "Piranha" (a mixture of sulfuric acid and hydrogen peroxide) treatments in order to make the channel hydrophilic and so to be able to conduct liquid. The peroxide removes hydrocarbons contaminants while the sulphate ions remove metals by the formation of soluble complexes. The next step is to make electrical contacts to the detector and the antifuse by SiRN etching and metal deposition. A construction for the entrance and outlet of the channel is then realized.

To fill the channel, confinement of liquid at the channel ends is necessary. This was achieved by plasma deposition of a hydrophobic Fluor-Carbon layer in the form of rings onto the wafer using a shadow mask. The Fluor Carbon layer is made from the plasma of CHF_3 at a flow of 25 sccm corresponding to a pressure of 150 mTorr. The process would be completed with the etching and metallization of the backside.

VI.3 Device properties

The completion of the device demonstrates the possibility of completely integrating a microfluidic component with IC circuitry in standard silicon processing. The working dimension of the device is structured vertically instead of laterally [7]. The novelty of this structure is the omission of a waveguide in optoelectronic/fluidic sensing systems [8]. In this way, it is clear that the coupling losses and losses within the fiber are avoided in the optical path. However, other minor optical losses are present due to the difference of refractive indices of the layers.

VI.3.1 Electrical

To verify the novel integrated device, electrical measurements on its components were carried out. In Figure VI.3-1, the pre-breakdown current voltage characteristics of a capacitor are shown for both biasing polarities. It shows the well-known Fowler Nordheim tunneling at the biased voltage of 7 V. At lower field, the leakage current has been observed to be in resemblance to standard thin oxide MOS capacitors. Therefore these pre-devices are good enough for the formation of the antifuses.

In order to create the antifuse, the same procedure as that described in chapter II is used, a constant current of 100 nA stresses the capacitor until oxide breakdown with positive bias on the upper p-type polysilicon electrode.

Further programming currents up to 5 mA were then applied. In reverse breakdown condition, the diode antifuse emits visible light. The current voltage curve of the antifuse is plotted in Figure VI.3-3 showing an electrical breakdown at less than 3 V. The mechanism of the breakdown is Zener breakdown due to the highly doped level of both electrodes. The series resistance has not been improved compared to the device reported in [1]. The measured series resistance of ~3KΩ come mainly from the spreading resistance of the antifuse (a point contact has a spreading resistance $R_{sp} = \frac{\rho}{4r}$, ρ –resistivity and r – contact radius); the sheet resistivity of the n-poly electrode is 30 Ω/□ and 60 Ω/□ is the value for the p-poly electrode, while the antifuse size radius is taken about 50 nm. For a better efficiency of the emitter, the poly-electrodes in future devices should be further optimized.

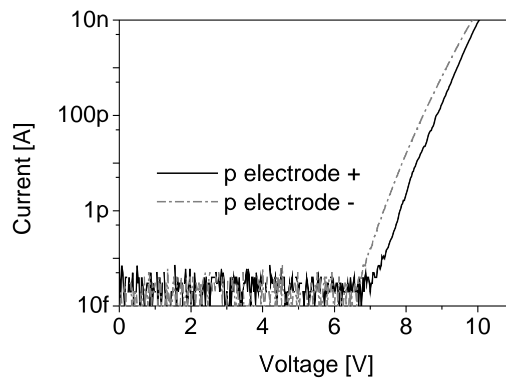

Figure VI.3-1. Pre-breakdown current voltage curve of the antifuse capacitor in both biasing directions

The opening of the contact hole to the buried photodetector was of poor quality due to the difficult etching of 1.5 μm thick SiRN layer. The photodiode current voltage characteristics show high reverse leakage current and enormously high series resistance (Figure VI.3-3).

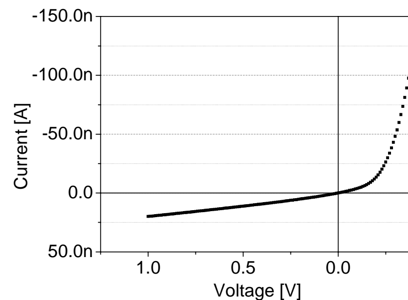

Figure VI.3-2. Photodetector I-V characteristic in dark

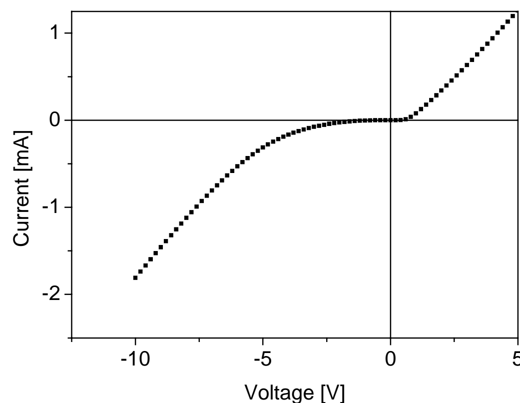

Figure VI.3-3. Current voltage characteristics of this diode antifuse

VI.3.2 Optical

To understand the effect of the channel on the optical properties of the antifuse, the spectra were measured by collecting emitted photons from the front side of the device with a fiber optical probe. The output of the optical probe is connected with an Avantes AVS-SD2000 spectrophotometer, which is controlled by a computer with measurement data displayed instantly.

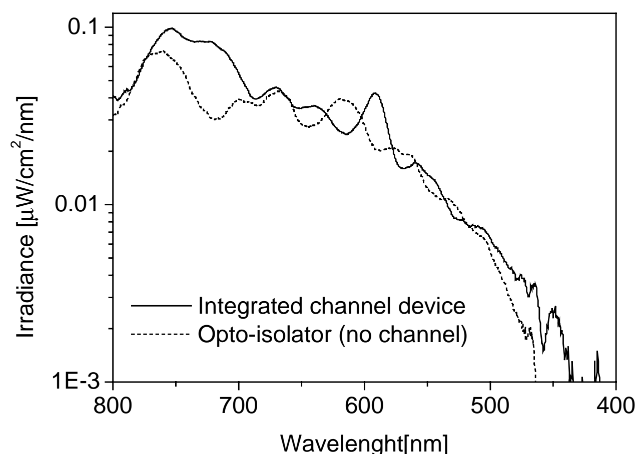

Figure VI.3-4. Semi-log scale spectrum of the antifuse at I_r =1.2mA as the channel is unfilled compared to opto-isolator device

The spectrum at antifuse current of 1.2 mA is displayed in Figure VI.3-3 showing the interference fringes of the emitted light waves due to the multi-layer structure of the device. The fringes have been previously observed in simple poly/mono antifuse structure, where the interference originates from the stack of oxide/poly-Si/air (chapter III). The position of these extremes versus wavelength could be displaced by changing the index of refraction of one or more layers or by changing their thickness. In the present case, the pattern is more complicated with pronounced peaks and dips. Figure VI.3-3 also compares the curve measured from the opto-isolator device (chapter V) with the one measured from this integrated device while the channel is unfilled. The difference is inherent due to the two different integration processes with difference properties of layers.

Filling the channel with other materials instead of air allows experiments on modulating the characteristic fringes.

Materials	Index of refraction
Air	1.000
Water	1.330
Ethanol: Water 75:25	1.361
Glycerine	1.473

The channel was filled with de-ionized water, aqueous glycerine and an ethanol: water (75:25) mixture. Measured spectra were recorded at 1.2 mA reverse biasing current of the light emitting antifuse and were compared with the spectrum of an unfilled channel. The shift of the extremes is clearly seen as shown in Figure VI.3-5. The displacement of the extremes are dependent on the complex refractive index of the material filling the channel, and can be calculated theoretically by multi-layer physical optics formulations [9]. The spectrum measurements of the unfilled channel were repeated after emptying the channel showing consistent shape and slope. It is clear that this device poses potential applications in sensing metrology for microfluidics.

In Figure VI.3-5, the curve for water has been chosen as the reference curve. It is clear that the larger the difference of refractive indices, the more pronounced deviation from the reference. The small $\Delta n \approx 0.031$ between water (n=1.33) and the ethanol: water mixture (n~1.361) results in almost identical spectral interference curves with little peak displacements. The

accuracy of the measurement setup jeopardizes our discussion on the intensity difference.

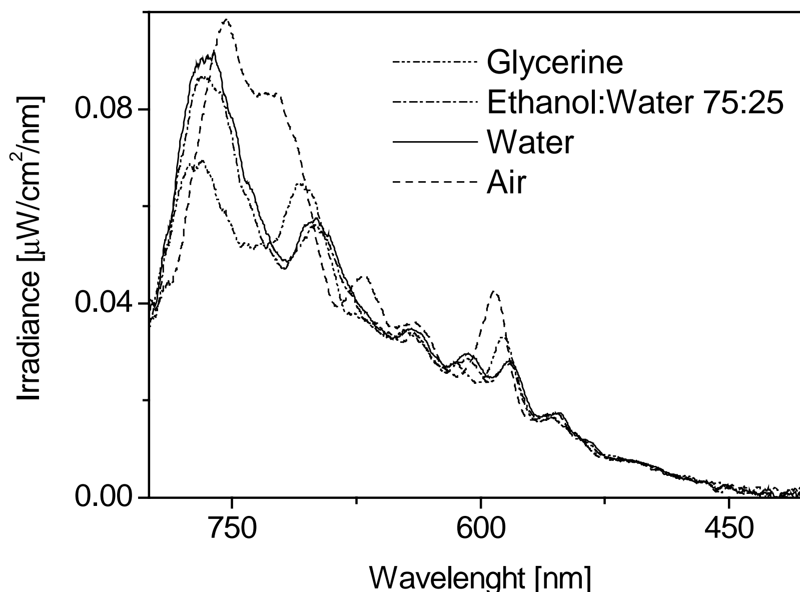

Figure VI.3-5. Spectrum of the antifuse as the channel is filled with other materials

VI.4 Discussion

As has been discussed in section VI.2, the channel of the device was made by wet chemical etching in KOH, a not very CMOS friendly solution. An immediate possible replacement is Tetra Methyl Ammonium Hydroxide (TMAH), which is an IC compatible etchant. Moreover, the addition of 1.4 wt.% (or more) dissolved silicon and 0.4± 0.7 wt.% $(NH_4)_2S_2O_8$ ammonium peroxodisulfate to a 5 wt.% TMAH solution [10] would reduce the aluminum etching rate of this solution to almost zero, which allows post-metallization processing of the channel.

Another limitation of the current approach is the treatment in "Piranha" solution. This step has to be done to restore the hydrophilic properties of the channel walls, which allows the conduction of liquid in the channel by capillary forces. This treatment step has also to be replaced by an aluminum friendly solution. Nevertheless, if TMAH etchant is used, this chemical is

gaseous at room temperature, which means no residuals will remain inside the channel upon drying [7].

The liquid flow speed measurement and absorptivity are other possible applications of this device. At a fixed light emitting current, the change in the medium of the channel can be sensed on the detector by the alteration in the magnitude of the photocurrent. This alteration is caused by the absorption of photon in the liquid that fills the channel, and the new refractive index difference at the two interfaces of the channel walls [1]. The absorption by the channel material can be calculated easily with empty channel (reference signal) and filled channel as the photodetector is improved. This experiment was not implemented due to the problematic metal contact to the detector.

This device has many potential applications by introducing some modifications and improvements of the structure.

- A filter stack on top of the detector can be integrated so as to let only a certain part of the spectrum pass.
- The device becomes much more sensitive to refractive index changes when the "thickness" or "height" of the hollow channel increases.
- Different channel height on the same device with multiple emitters and detectors, which would allow more precise calculation of the refractive index.

Other ways to improve this device are dependent on the specifically desired applications.

VI.5 Conclusions

The success of the novel device indicates that a system of light emitter, photodetector and a reaction chamber, a microchannel in this case, can be fabricated on silicon with IC technology. For the first time, nanometer-scale light emitting diode antifuses have been applied to a microfluidic device. The electrical and optical properties of the components prove the feasibility of the combined technologies and the working principle of the integrated sensor system.

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Chapter VII

INFRARED EMISSION FROM FORWARD-BIASED SILICON DIODE

Novel approaches

In this chapter two newly developed processes for silicon infrared light emitting devices are presented, namely the dislocation loop engineering diode and the lateral P-I-N junction device on SOI wafers. The characteristic emission around the silicon band was recorded showing a high external quantum efficiency of around 0.025 to 0.1 %. For the dislocation loop engineering devices, there is a conformable relationship between the emission intensity and the device temperature. This fact has never been observed in other silicon light emitting systems. The lateral P-I-N diodes realized on SOI wafers demonstrate the same efficiency and a significantly wider Full Width at Half Maximum emission spectrum compared to the bulk device.

VII.1 Introduction

The mainstream throughout this thesis, until this point, is the concern with the visible light emitting antifuse devices working in reverse biased breakdown condition. The subject discussed in this chapter, however, differs from the previous ones, since an investigation on two new devices functioning in forward biasing condition, with peak emission in the infrared region [1][2], will be presented. The chapter shows experimental results on optical and electrical characterization of dislocation loop devices and lateral PIN diodes formed in SIMOX SOI (Separation by IMplanted OXygen Silicon On Insulator) substrate. They were found to emit characteristic silicon band gap infrared light with reasonably high efficiency. While the antifuse has been oriented for application in sensor systems, these devices are more suitable for realizing on-chip and inter-chip interconnections. They seem to be the most probable structure for integration with silicon-based waveguides and photodetectors.

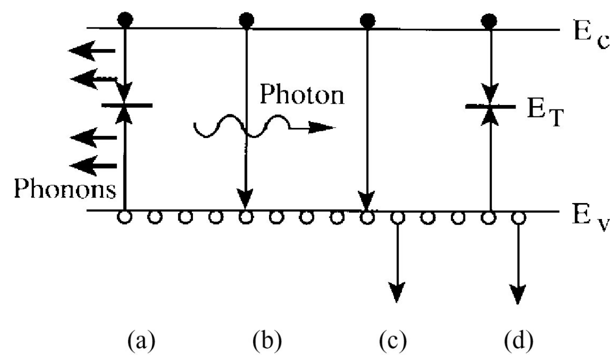
Silicon based optoelectronics suffers from the absence of a true silicon light source. Emitting efficiency of around 1.0 % close to room temperature was reported in [4], which improved the efficiency by reduction of internal reflection using texturized emitting surface and antireflection coating, but such a device had some inherent weaknesses, especially the feasibility to be integrated in an all silicon optoelectronic system. Meanwhile, for on-chip optical interconnects the CMOS integration and the interface to wave guiding medium are the key issues. The modulation of the light source for fast signal transmission and communication is another subject that must be solved. The long carrier lifetime of radiative recombination in bulk silicon is in conflict with fast switching requirement.

It has been known that silicon is a very poor light emitter. However, according to the theoretical calculations in [3], quantum efficiency of interband radiation in highly purified silicon with low concentration of deep impurities and defects can exceed 10 % at room temperatures in the case of negligibly small surface recombination. This value can be reached on the basics of a large bulk SRH (Shockley-Read-Hall) lifetime as well as negligibly weak impurity assisted Auger recombination in a perfect crystal. The authors also claim that in such a condition surface recombination is responsible for the low value of quantum efficiency and suggest that the best quantum

efficiency values can be obtained in $Si\text{-}SiO_2$ structures with low density of surface states.

The radiative recombination (b) in silicon is a phonon mediated indirect transition process. The probability for a photon emission is therefore dependent on the availability of a phonon with appropriate momentum and energy. It is understood that the transition assisted by phonon emission is more probable due to a negligible amount of phonons suitable for absorption at room temperature [4]. Meanwhile, in bulk silicon, other recombination processes like Shockley-Read-Hall (SRH) (a) and Auger (c, d) are competing.

Figure VII.1-1. Recombination mechanisms: (a) SRH, (b) radiative, (c) direct Auger, and (d) trap-assisted Auger. (after [6])



Each process has its own characteristic lifetime and makes up the effective lifetime of the material:

$$\tau = \frac{1}{\dfrac{1}{\tau_{SRH}} + \dfrac{1}{\tau_{rad}} + \dfrac{1}{\tau_{Auger}}}$$

Radiative recombination is important in direct bandgap materials like GaAs and InP, where the conduction band minimum lies at the same crystal momentum value as the valence band maximum. During the recombination event, phonons are not required, since the energy is completely dissipated by the emission of photons. On the contrary, radiative recombination in Si has been almost neglected because of the considerably long lifetime.

From these arguments, it is clear that if the non-radiative recombination routes are depressed, the radiative recombination can be enhanced

consequently. This can be done by making $\tau_{rad} \sim \tau_{SRH}, \tau_{Auger}$ or the other way around. In bulk silicon, following approaches could be attempted:

i. Block the diffusion of carriers to point defects where trap-assisted recombination dominates

ii. Lower the carrier mobility by potential barriers or small structures

iii. Reduce free carrier absorption by using moderately doped wafers and heavily doped regions are confined to small volumes

These approaches clearly attempt to render τ_{SRH}, τ_{Auger} to higher values only, which do not improve the speed for radiative emission. Nevertheless, the present concern concentrates more on the efficiency improvement. Thus, in this chapter, two different approaches have been implemented tackling the low emission efficiency in silicon: the dislocation loops engineering diode (DILED) and the lateral diode realized on Silicon On Insulator (SOI) material (LATODE). The former employs the first approach and the latter, to some extent, employs the next two approaches.

VII.2 Dislocation loop LED (DILED)

The dislocation loop device, first proposed by [10], features the introduction of dislocation loops into the region close to the junction as means of promoting radiative recombination. The array of dislocation loops is generated because of the ion implantation and high temperature treatment processes in IC technology. The array of loops induces a local spatial strain field, which forms a spatial potential barrier. This potential barrier effectively confines the free carriers, blocking them from diffusion to point defects [10]. The strain at the edge of the loop is high and falls off around each loop approximately with the inverse of distance [18].

Dislocation loops are, in fact, unwanted defects in silicon processing that uses ion bombardment techniques. Unfortunately, ion implantation is the primary source of introducing impurity atoms into silicon substrate. The ion implantation process causes a large amount of crystal damage and creates defects. The damage can be largely repaired during subsequent annealing steps. However, if the implant doses are high enough, extended defects such

as dislocation loops and {311}'s defects [12][13] are formed during these heat treatments.

The presence of dislocation loops will increase the leakage current and affect the final properties of devices if they are located at or near the device junction, especially in the depletion layer of a junction. Increased leakage current will cause device degradation and increased power consumption in logic and memory circuits. On the other hand, the device is not affected if the dislocations are outside of the space charge regions. For promoting radiative recombination, the array of dislocation loops should belong to the latter case.

This experiment aims at examining the results of [10] and investigates the device dependences on annealing temperature and elevated substrate temperature above 300 K.

VII.2.1 Device realization

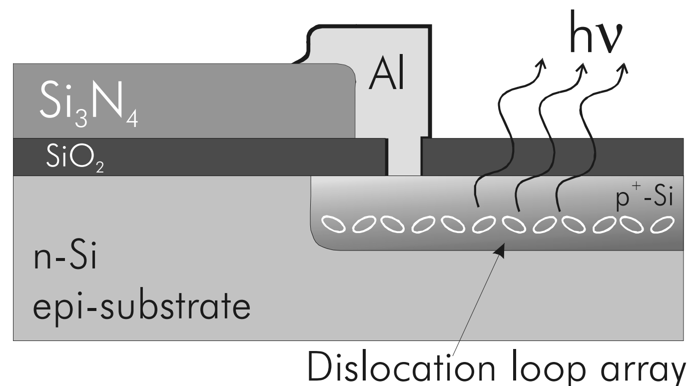


Figure VII.2-1. Dislocation loop LED device sketch

A simple diagram of the device is shown in Figure VII.2-1. The p^+ region was made by implantation of boron at a dose of 1.0×10^{15} cm^{-2} and at an energy of 40 keV. The samples were subsequently annealed in a nitrogen atmosphere for 20 minutes at 850, 900, 950, 1000, and 1050°C respectively to form the dislocation loop array and to activate the boron atoms. The implants were made into device grade epitaxial n-type silicon substrates of resistivity 2.55÷2.95 Ωcm with the epi-thickness of 16÷18 μm. Front side metallization for electrical contacts was made by aluminum sputtering and sintering in wet nitrogen ambient at 400°C for 5 min.

VII.2.2 Results and discussion

Electrical characteristics

For electrical measurements and supply, an Agilent 4156B precision parameter analyzer [14] was used. Current voltage characteristics (I-V) of the devices plotted in semi-log scale are shown in Figure VII.2-2. The reverse biased region indicates very low leakage currents, an evidence of no dislocation loops present at the junction space charge region. In the forward biased low injection regime, it is noticed that the diffusion current conduction is the dominant mechanism of this device, signifying the recombination outside of the space charge region.

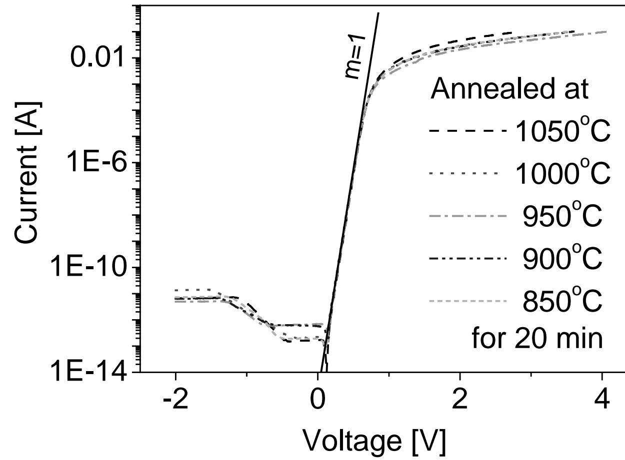


Figure VII.2-2. I-V curves of the DILED's shown with $\sim e^{\frac{qV}{mkT}}$ (m=1)

External (quantum) efficiency

The emitted photons are collected from the front side window of the device with a fiber optical probe. Light emission spectra are measured from the output of the optical probe with an Instrument Systems Spectro–320 universal spectrometer and/or an Avantes AVS-SD2000 spectrometer. A calibrated halogen lamp HL-2000 has been used as reference for absolute measurements. Both spectrometers are computer interfaced and controlled (Appendix B).

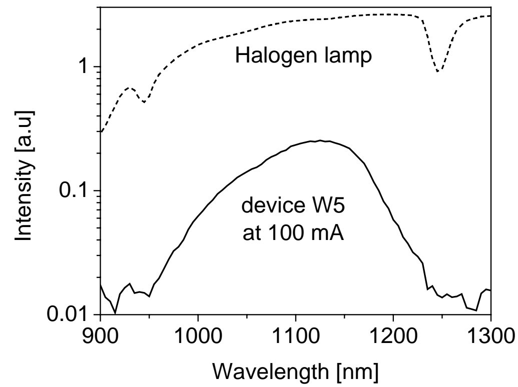


Figure VII.2-3. Irradiance intensity compared to calibrated halogen lamp

Figure VII.2-3 shows a comparison between the spectrum of the halogen lamp and the spectrum of device W5 (1050°C, 20min) operated at 100mA emitting current. The irradiance output intensity of the calibrated lamp is known at a distance of 1 cm away from the lamp bulb. The ratio of peak intensity gives an order of magnitude higher for the halogen lamp (5V, 1.4 A).

Due to the nature of the measurement system with the optical fiber probe, the external efficiency is based on the power density of the emitted photons and electrical power density of the current through the device, namely, $\eta = \frac{P_{optical}[W/cm^2]}{W_{electrical}[W/cm^2]}$ (Figure VII.2-4). The electrical power density is the quotient of the power dissipated through the device and the device surface area. The division of collected optical power over the fiber entrance area, on the other hand, gives the estimation of the optical power. Taking into account the error margin, a value close to 0.1 % is obtained, which is similar to the value reported in [10], the first article that discussed the effect of dislocation loops. The device discussed in this chapter, however, has reverse biased currents in the nanoampere range compared to that of reference [10] with 0.5 mA at reverse bias of −2V. It is very probable that their device suffered from the presence of dislocations at the junction.

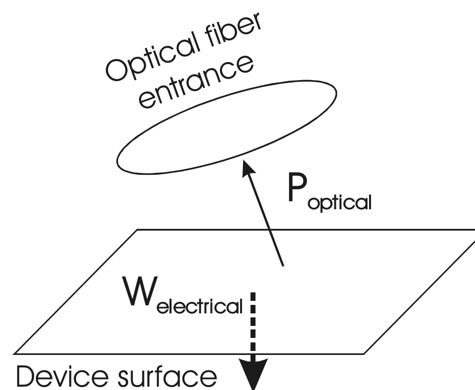


Figure VII.2-4. Schematic illustration for the estimation of external efficiency

Current dependence

In Figure VII.2-5 (a), emission spectra at three different forward currents are displayed. The dependence of peak intensity on current in Figure VII.2-5 (b) is plotted in the logarithmic scale, showing a linear correlation. It has been argued that this behavior is quadratic because the recombination involved both electron and hole. However, a linear dependence is supported here, which bases on the fact that radiative recombination takes place in the region where either electrons or holes form a strong majority [4], the implanted p-region in this case where holes concentration is dominating.

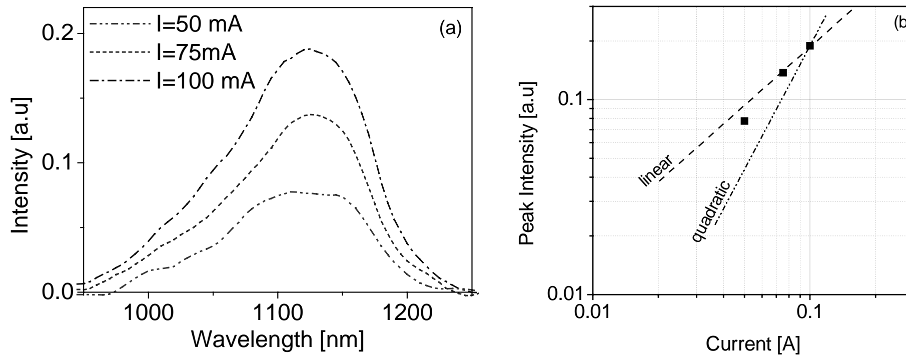


Figure VII.2-5. Current dependence behavior of the light spectra (device W4, 950°C, 20 min)

Substrate temperature dependence

There is an increase of EL intensity with increasing substrate temperature even at above room temperature, which is a striking contradiction to most of other systems that were demonstrated for light emission in silicon including erbium doped silicon, iron di-silicide.

The temperature dependence of the device annealed at 1050°C is displayed in Figure VII.2-6. The temperature was varied from room temperature up to 473K (200°C). A slight increase in intensity is observed as the temperature is raised. A full understanding of this increase of the integrated intensity with temperature requires further investigation; it could be associated with increased scattering within the confined carrier populations and the increase in the effective density of band states with temperature [10]. On the other hand, the temperature dependence of the radiative recombination coefficient

of silicon is still not in consensus. In reference [11], though the authors proved that this coefficient is decreasing at higher temperature, the result was in disagreement with other two previous publications that were referred to.

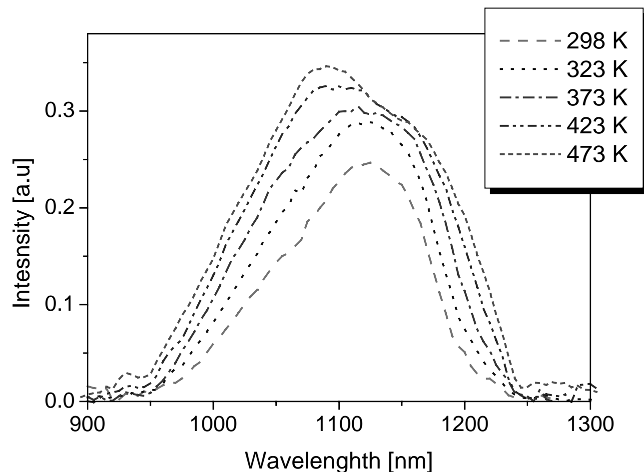


Figure VII.2-6. Substrate temperature dependence of emission spectra of device W5 at I_f=100 mA

The temperature at which the electroluminescence saturates has not been identified (out of reach of our temperature system) but the increase levels off above 423 K (150°C). It is obliged to stress here that the spectra at substrate temperature of 423 K and 473 K (150°C and 200°C) have an indent around the peak of intensity. The tentative explanation for these abnormalities will be discussed in conjunction with the SOI device mentioned later in section VII.3.2.

Annealing temperature dependence

The different annealing temperatures vary the boron diffusion profiles as well as the evolution of the dislocation loops and other defects. In Figure VII.2-7, the emission spectra of devices annealed at four temperatures are displayed. The best result is achieved on devices annealed at 1050°C. The trend still continue at 1050°C, however, we suggest a weakening luminescence of devices fabricated at higher annealing budget due to the complete dissolution of loops at above 1100°C [15].

The intensity increase can be attributed to the evolvement of the loops with annealing temperature, since time is kept constant. Due to the importance of implantation technique in IC-industry, all aspects of this method have been researched intensively, in which much work has been dedicated to the study of the evolution of dislocation loops leading to an immense understanding on this subject [15][16][17]. The explanation of the increased intensity, based on the vast literature available on dislocation loops, is presented as follows.

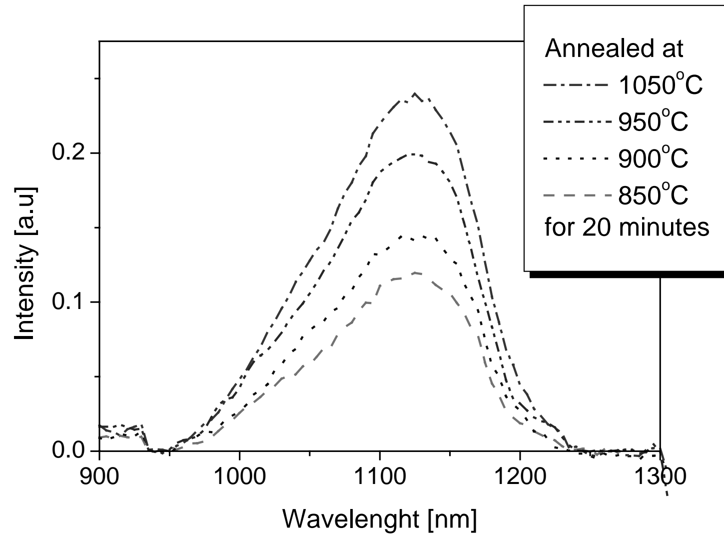


Figure VII.2-7. Increased emission with higher device annealing temperature

Temperature	*Loop trend vs. time*				
(°C)	Average radius (nm)		Density (cm^{-2})		Mode
700	~4	→	~5×10^{11}	→	not pronounced
800	~6.5	→	~2×10^{11}	→↘	coarsening process begins
900	~9.5	↗	~1.1×10^{11}	↘	pronounced coarsening
1000	~25	↑	~1×10^{10}	↓	loops grow in size and density decreases
>1000	dissolution process of loops				

The presence of dislocation loops induces a local strain field in the silicon lattice, which is found to be strongly sensitive to the size and density distribution of the loops. Thus, density and size of loops govern the evolution of the strain field that determines the spatial potential barrier for the

confinement of free carriers. The dependence of loops with temperature can be generally classified as in the above table (experimental data from [16]).

According to reference [17], the average loop radius, which is an indicator of how large the loops are, is important in relating the spread of the strain in the lattice. The larger the loop, the larger is the length of the strained lattice. The larger strained lattice contributes to the improved potential barrier, which is the reason for the increased intensity in Figure VII.2-7.

VII.3 Lateral PIN diode (LATODE)

The use of SOI material for realization of silicon light emitters is also based on the idea of introduction of potential barriers into the light emitting active region. The isolation of the thin silicon sheet (called device layer) from the bulk by the buried oxide (BOX) layer is very appropriate for that purpose leading to the realization of the device described in this section.

SOI material has gradually increased its role in modern IC industry thanks to its clear advantages over standard conventional silicon wafers [7]. An SOI substrate consists of a thin single-crystal, defect-free sheet of silicon sitting on top of an insulator. It has been produced by a dozen of techniques; SIMOX is one among those methods [8]. The decrease of oxidation rate of the thin silicon layer, discussed in [9], as this layer is being thinned down to the first silicon/BOX interface is very suitable for silicon quantum device fabrication. The separation of devices from the substrate underlies the capability of faster optical modulation. The device, discussed in the following, takes the advantages of SOI wafers to implement the approaches that were mentioned in section VII.1.

VII.3.1 Experimental

The starting material is 4-inch SIMOX SOI substrate, with silicon layer and buried oxide (BOX) layer thickness of 190 nm and 350 nm, respectively. The device layer is p-type silicon with a resistivity of 20 Ω.cm^{-1}. First, device layer is etched into different islands, on which PIN diodes with different structures will be realized, by a selective etching in TMAH. The PIN neutral region has different thicknesses d_{Si}, of ~10 nm on devices with the intermediate oxidation step and of ~180 nm on devices without this oxidation. Implantation of BF_2^+ and As^+ with doses of 3.10^{15} and 5.10^{15} respectively,

were used to fabricate the highly doped p-type and n-type regions. These heavy doping regions are localized to contact areas. Dopant activation was processed by a furnace anneal at 1000°C for 30 min. Metal contact areas are small and were fabricated by sputtering of Ti/W barrier layer and Al (+1 % Si) on the wafer after contact holes had been opened in the BPSG interlayer.

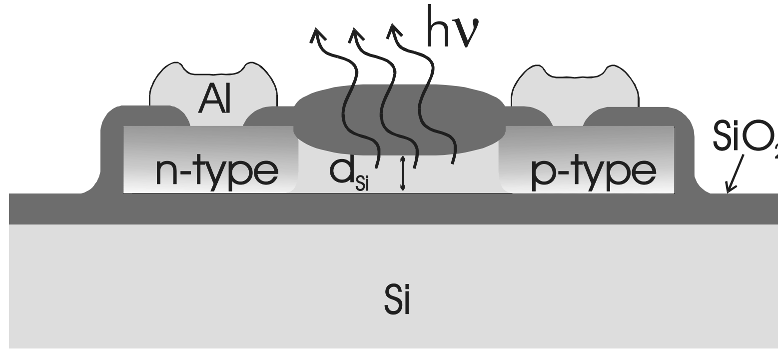


Figure VII.3-1. Schematic drawing of the device

VII.3.2 Results and discussion

Electrical characteristics

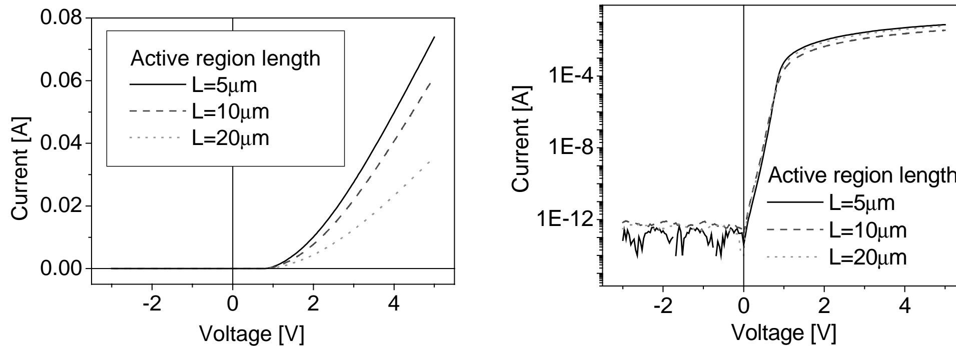


Figure VII.3-2. I-V characteristics of devices with different active regions lengths in linear and semi-log scales

Lateral PIN junctions formed in SOI structures exhibit good current voltage (I-V) characteristics with very low leakage current. Saturation current density of 3.10^{-11} A/cm^2 and ideality factor of 1.3-1.5 were found in these junctions. A 100 mA forward current can be reached at 4.16 V on the shortest neutral region structure. The neutral region width and length determine the resistance

of the structure. I-V characteristics for the different geometries of the devices are displayed both in linear and semi-log scale in Figure VII.3-2.

Optical properties

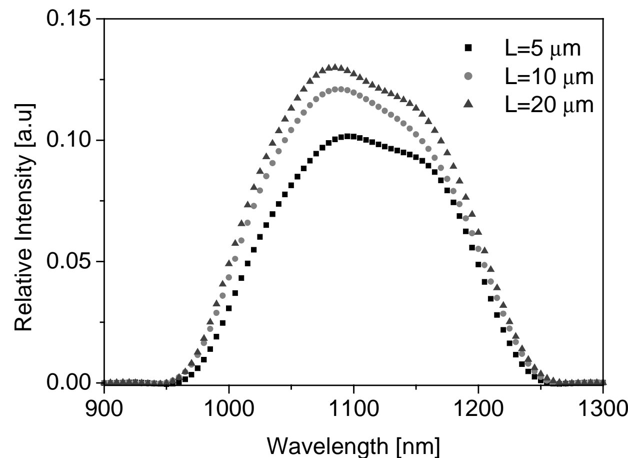


Figure VII.3-3. Emission spectra of lateral diode devices with three different active lengths

In Figure VII.3-3, three spectra of devices emitted at the forward current of 100 mA with different active region lengths are displayed. The difference in intensity is attributed to the emitting area of each device being seen by the aperture of the optical probe. The quantum efficiency of the device cannot be calculated explicitly, however, it is in the same order as that of the dislocation loop device (see Figure VII.3-4). It is also worthwhile to note that the top oxide thickness on this device has not

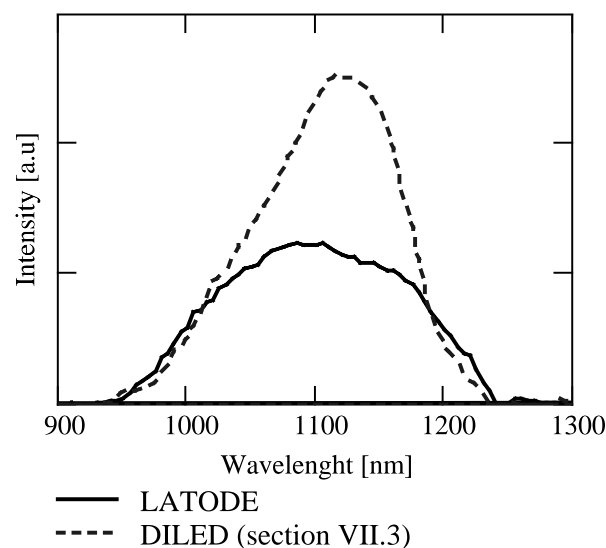


Figure VII.3-4. Spectrum of the LATODE device compared with that of the DILED

been optimized for maximum transmission.

The emitted spectra cover the wavelength range from 950 nm up to 1250 nm with a Full Width at Half Maximum (FWHM) of 0.202 eV. This value of FWHM is significantly larger compared to the bulk emitting devices (Figure VII.3-4).

As the device is biased deep into ultra-high injection condition a weak visible emission peak at 720 nm is observed (Figure VII.3-5), however, the device is working in a very unstable state. The origin of this peak is not clear and will not be discussed further.

The SOI devices with very thin active region (<10 nm), as mentioned above (section VII.3.1), were manufactured with an intermediate oxidation process. This device shows even wider FWHM (Figure VII.3-6), which probably feature a deformed energy bandgap with quantum mechanical consequence. However, this effect needs further investigation.

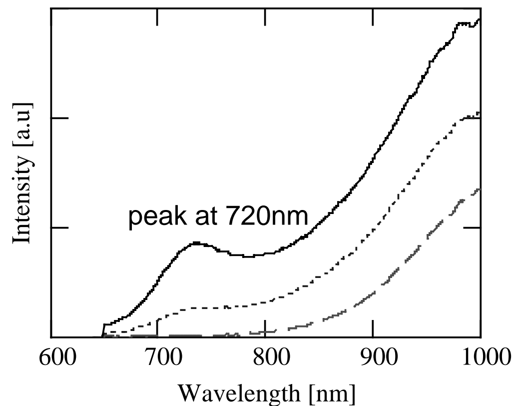


Figure VII.3-5. The visible emission peak at 720 nm (dark solid line) under ultrahigh injection condition

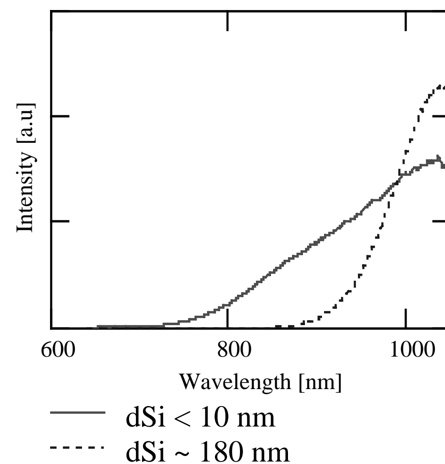


Figure VII.3-6. Emission linewidth broadening of ultra-thin active region LATODE (d_{Si}<10 nm)

This device structure also can function as a photodetector when it is operated in reverse bias. The photon-induced currents for each active region length at

three illumination levels are plotted in Figure VII.3-7 showing the linear dependency on area. The larger the active region length, the more light is absorbed and thus more current. However, in this measurement, the illumination was with visible light from a tungsten lamp. If photodiode detectors capable of sensing the emitted signal can be realized in parallel, this system will be brought closer to real applications. In that fulfillment, heavily doped silicon photodetector can be introduced. The degenerate states of doping impurities lower the bandgap by merging with the conduction band minimum or valance band maximum. In this way, silicon can absorb more infrared emission that is usually transparent. Another approach that can be used is the photodetector with a resonant cavity [19]. This device features the so-called Distributed Bragg Reflector (DBR), which is a two period Si-SiO_2 structure realized on SOI wafers, performing as a 90 % reflecting surface.

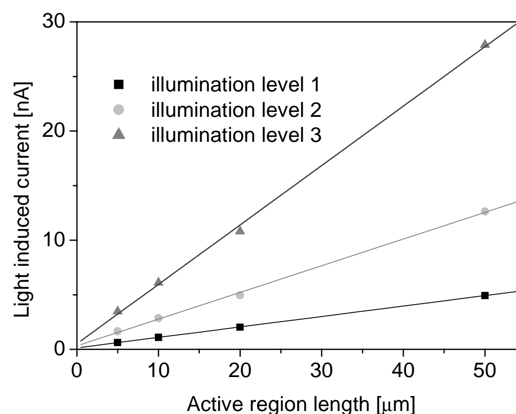


Figure VII.3-7. Light induced currents of structures with different active region length

Discussion

In Figure VII.3-3, there is an indent at wavelength of 1130 nm of the spectra, which looks similar to the high temperature emission of the dislocation loop device (Figure VII.2-6). Such a coincidence is probably caused by the self-heating of the thin silicon layer. The reasons for the presence of the indent at high temperature as well as the increased intensity at higher substrate temperature in dislocation loop device are still not clear. The indent might have its root from the increased absorption of the silicon at higher temperature at that wavelength, as discussed below.

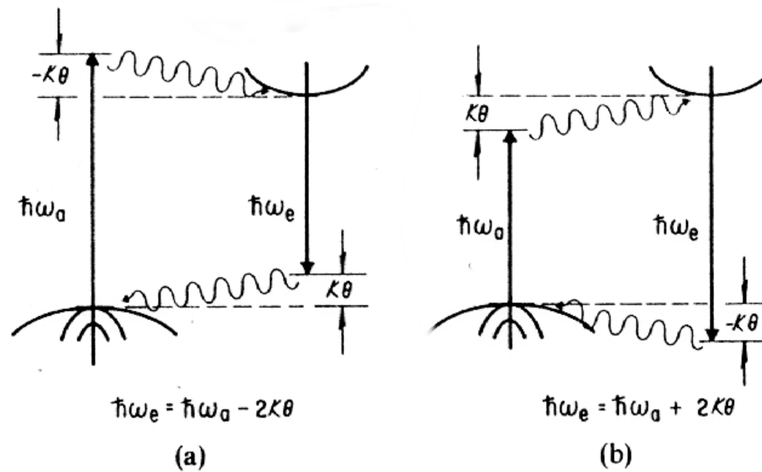


Figure VII.3-8. Comparison of indirect absorption and emission processes involving either phonon emission (a) or phonon absorption (b) (after [20])

At room temperature, it has been previously mentioned that the radiative emission process assisted by a phonon absorption event is negligible, however, as the temperature rises, it can no longer be ignored probably due to the increased population of phonons with energy suitable for this radiative route. Along with this emission process of photon is the photon absorption process also mediated by phonon absorption, which has $\hbar\varpi_a + K\theta \approx \hbar\varpi_e + K\theta$ (Figure VII.3-8). The result of the competition between these two conflicting process might be the cause of the indent at high substrate temperature dislocation loop device and for the SOI devices.

The wider FWHM of the Lateral SOI diode can be attributed to the self-heating temperature rise. The free carriers both on conduction band and valance band have $\sim 3kT/2$ thermal energy. The difference of FWHM is about 0.1 eV. That means the lattice temperature of the lateral diode should be around 413 K (140°C). This value corresponds closely to the appearance of the indent on the dislocation loop device spectrum at the temperature of 150°C (Figure VII.2-6), which also shows up in the spectra of the LATODE.

VII.4 Conclusions

Two approaches for realization of efficient silicon LED have been presented. The dislocation-loop engineering device has the advantage of strict

compatibility with IC standard technology as well as simple fabrication process. It also offers efficient operation at room temperature and above. The lateral diode on SOI features a wider FWHM spectrum. This device poses a potential integration of an all-silicon on-chip optical interconnection scheme with light emitter, waveguide, and detector. The capability of fast modulation is also a topic for further investigation.

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Chapter VIII

CONCLUSIONS & RECOMMENDATIONS

VIII.1 Conclusions

Chapter II and III

Three most crucial properties of the diode antifuses, namely electrical, optical and structural have been investigated and discussed. The formation of the antifuse using electrical fusing of a thin dielectric capacitor has also been described. The physical structure of the antifuse has been exposed. It is clear that the antifuse sizes are of nanometer-scale range e.g. about a few tens of nanometers. The electrical characterization indicates that antifuses are reproducible in the aspects of yields and stability. The emitted light spectra from the antifuses in reverse bias have been studied and formulated with a multi-mechanism model, which has been proven to be applicable for conventional diodes. The distinguished difference in the model parameters is the higher electron temperature and stronger electrical field strength, which are achievable only in nanometer-scale devices like the antifuses. The lowly doped substrate device shows a forward biased light spectrum with a tail extended deeply into the visible range. This anomalous light spectrum is attributed to the electron tunneling through oxide.

Chapter IV

An example of using ultra violet photons emitted from an antifuse diode for a photochemical process is described. It has been made clear that microscale chemistry is enabled with this device. Photoresist has been employed as the chemical medium. A technique for IC reliability testing is proposed based on the content of this chapter.

Chapter V, VI

The antifuses were realized in a new manner, i.e. oxide breakdown between two layers of oppositely and highly doped polysilicon electrodes. They have been integrated into the two novel devices, the opto-isolator (*chapter V*) and the channel device (*chapter VI*).

The opto-isolator demonstrates the antifuse as an efficient visible light source and the feasibility for integration with silicon IC. The differential reflected photons at the front surface could be sensed with the integrated photodetector, suggesting the use of this integrated device as an optical sensor and actuator element. The device resembles optoelectronic interconnections for intra-chip communication, though the coupling of the emitted optical signal to a waveguide in practical devices is still the predictable obstacle.

Chapter VI presents a novel concept of an optical microfluidic device. The light emitting antifuse and the photodiode have been integrated with a hollow channel, enabling fluidic experiments on an all silicon device. The channel's influences on the transmitted spectra of the antifuse have been recorded as it is filled with liquids of different refractive indices. This device poses potential applications in microfluidic metrology.

Chapter VII

In this chapter, two silicon devices for highly efficient light emission working in forward biased mode are investigated and evaluated. The DILED featuring the engineered junction with dislocation loops demonstrates efficiencies approaching 0.1%. The device possesses a precious property; the conformal intensity increase with higher substrate temperature that has never been observed in other silicon based light emitting systems. It has also been shown that appropriate annealing budget improves the device efficiency. The LATODE device, based on SOI wafer, shows distinctive emission spectra with wider FWHM compared to bulk devices. The structure is a potential candidate for on-chip all-silicon optical interconnects due to its efficiency and prospective integration capability.

VIII.2 Recommendations

The light emitting antifuse

The research toward the applications of antifuses might be extended to the incorporation of other materials with proved optoelectronic properties such as GaN, SiC to examine the possibilities of efficiency improvement and to move the spectrum to deeper ultraviolet (UV) region where more applications in (bio)-chemical processes are possible.

Further understanding of the visible light emitted from LDS devices under forward bias is another area for accomplishment.

The microfluidic device

It is clear that the optical/fluidic device, described in *chapter VI*, has many prospective applications. With little improvement, the device will be capable of an absorption type optical sensor. Further modifications can be made to turn the device into a complete metrological system for microfluidic measurements.

The infrared emitter

A step forward to realization of optical interconnects on silicon is to develop a silicon based photodetector that is more sensitive to the wavelength of 1100nm. The improved efficiencies of the emitters and device structures in *chapter VII* are a good start for this direction, though the emission efficiency and the fast optical signal modulation are expected to improve further. Better understanding of the efficiency improvement mechanisms of the two devices discussed in *chapter VII* is also desired.

SUMMARY

Devices made from silicon dominate the microelectronics industry, thus silicon is the material of choice for anyone designing new electronic devices that will be integrated with microelectronic circuits. The same applies to the optoelectronic devices that act as gateways between the electronic domain and the worlds of photonics and optical communications. Most optoelectronic components, such as waveguides and modulators, have already been made from silicon, but a completely silicon-based system remains difficult because there is a critical missing link: a silicon light source.

Silicon has an indirect energy bandgap which means that the minimum in the energy of the conduction band and the maximum in the energy of the valence band occur at different momenta. Electrons and holes can only recombine if a lattice vibration (phonon) with the correct momentum is available. Therefore, silicon is fundamentally a very inefficient photon emitter. However, the huge benefits that silicon optoelectronics might bring motivate the growing research on this area. An efficient and fast light emitter realized on silicon with silicon technology is the conclusive goal.

This PhD research is among those attempts to strive for a silicon light source though the target is rather in sensor and actuator applications than optical communications. It deals with the development of a novel device, the nanometer-scale silicon light emitting diode antifuse. The objectives set out for the research were to investigate the device properties and the possible applications as an optical sensing and/or actuating element, especially in Micro Total Analysis (μTAS) or lab on a chip.

The thesis starts with an introduction on the properties of the silicon material with respect to light emission, namely, why silicon is a poor photon emitter, the benefits of an integrated opto- and microelectronics. A small review on the "state of the art" development of the subject is presented, which addresses most current approaches with the respective successes and limitations of each. The motivation of this research is then discussed.

The nanometer-scale silicon light emitting diode antifuse operates in the reverse electrical breakdown, emitting a wide spectrum of visible and near UV photons. It is created by electrically fusing a semi-manufactured capacitor pre-device. The physical size of the antifuse is in the order of less than 100nm, which is a link through the dielectric of the pre-device. The link formed between the two heavily and oppositely doped electrodes behaves as a tiny p-n silicon junction. The emitted spectrum is modeled with a multi-mechanism formulation that was previously used for conventional diodes.

The near UV photons (from 2.7-3.1 eV) were used to conduct a photochemical process, namely the illumination of photoresist. Though the efficiency of the high energy photons is largely less than that of visible ones, the structure of photosensitive component in the resist still receives enough energy to chemically change, which make themselves either soluble or insoluble in the developer, dependent on the type of process used. A simplified model was made to simulate the time dependency of the process. It has also been proposed as a high-resolution non-destructive reliability testing method for VLSI integrated circuits.

A long tail extending deep into the visible region was observed in the forward biased emission spectra of the antifuse structure, which has lower substrate doping (LDS device). The origin of this visible light and the mechanisms involved were revealed based on the comparison with antifuse spectra of HDS devices. The discussion supports the transition of hot injected electrons into the conduction band of the Si-bulk of diode antifuses.

The antifuse was then integrated onto two novel prototype devices, the opto-isolator and the optical/fluidic device. The former consists of the light emitting antifuse and a photodiode detector that is integrated underneath. The optical/fluidic device has nearly similar structure, except for a microchannel sandwiched between the light emitter and the detector. The detection of the light signal on the detector of the opto-isolator was carried out showing an overall electrical efficiency of 10^{-6}; the power conversion efficiency was also roughly estimated. The isolator performed as a sensing element, however the signal seems still small for practical applications. The stability of the system was tested for a long period showing small degradation.

The channel of the optical/fluidic device were filled with different liquids that consequently altered the interference pattern of the light source proving the working principle. This device has a wide range of possible improvements and applications. It can be an absorption type sensor, a bubble creator, and a metrological measurement system for microfluidics.

The thesis also extends its content to the research on the improvement of efficiency. It describes two devices operating in forward biased regime. The efficiency of these devices is in the range of 0.1%, which is comparable to best devices reviewed in chapter I. The devices open up further chance of getting efficient and fast optical emitter on silicon, though intensive and in-depth investigation is still to require.

Finally, the thesis has created a strong basis for the development of nanometer-scale light emitting diode antifuse. Feasible prototype devices were developed with proved working principles. Infrared LEDs were realized showing promising characteristics.

APPENDIX A

CHANNEL INTEGRATED DEVICE

Process description of the device discussed in chapter VI

Phase/Step	*Process*
PHASE 1	Photodetector
14.	Wafer marking
15.	Standard cleaning
16.	Oxidation 300nm for the mask zero mark
17.	Definition of the mask mark for Mask I and II Lithography Mask O
18.	Wet etching of the mark definition
19.	25 nm pad thermal oxide – surface protection for implantation of boron
20.	Definition of photo detector windows Lithography Thick Olin 907–17 Mask I
21.	Boron implantation
22.	Resist removal & Standard cleaning
	End of PHASE 1
PHASE 2	Sacrificial poly-Si
23.	Standard Cleaning
24.	LPCVDeposition of 1st SiRN 0.5μm
25.	LPCVDeposition of sacrificial poly-Si 0.5μm
26.	Lithography for channel patterning Mask II
27.	Poly-Si dry etching preferably anisotropic
28.	LPCVDeposition of 2nd low-stress SiRN
	End of PHASE 2
PHASE 3	The antifuse
29.	LPCVDeposition of 1st electrode amorphous-Si 300nm (planar surface)
30.	B^+ doping by implantation

31.	Lithography Patterning of 1st electrode Mask III
32.	Resist removal and Standard cleaning
33.	LPCVDeposition of 60nm separation nitride
34.	Lithography Antifuse window opening Mask IV
35.	Standard cleaning native oxide removal 10 sec in BHF
36.	LPCVDepositon of thin antifuse oxide 8nm
37.	LPCVDeposition of 2nd electrode poly-Si 300nm
38.	Implantation of the second poly-Si layer
39.	Lithography Patterning of 2nd poly Si layer Mask V
40.	Lithography Patterning of the separation oxide Mask VI
	End of PHASE 3
PHASE 4	Hollow channel etching
41.	LPCVDeposition of covered low-stress SiRN 300nm
42.	Lithography Mask IX Making hole in SiRN
43.	Dry etching SiRN
44.	Resist Strip
45.	Sacrificial poly-Si etch in KOH
46.	Cleaning RCA-2 ($HCL/H_20_2/H_2O$)
47.	Cleaning "Piranha" (H_2SO_4/H_2O_2)
	End of PHASE 4
PHASE 5	Metallization
	Solution 1: Standard Technology
48.	Photolithography Definition of the contact hole Mask VII
49.	Dry etching of SiRN Selective to silicon recipe

50.	Fuming nitric acid for resist removal & SC
51.	Deposition of Aluminum by Sputtering
52.	Definition of Aluminum contact pad Lithography Mask VIII
53.	Wet etching of Aluminum in H_3PO_4
54.	Aluminum sintering
	Solution 2: Shadow mask solution
55.	Dry etching of SiRN using shadow mask
56.	Evaporate Aluminum using shadow mask
57.	Using steps 39÷41 to finish
	Solution 3: FIB
58.	FIB making contact hole
59.	Deposition of Platinum
	End of PHASE 5
PHASE 6	Deposition of liquid confinement ring
60.	FC deposition through shadow mask Elektrotech PF 310/340 (Etske) (CHF_3 flow 25sccm, pressure 150mTorr, power 20 Watt)
End of PROCESS	

Shadow mask fabrication

Step	*Process*
61.	Wafer selection (by curvature measurement)
62.	Standard cleaning
63.	Lithography Olin 907-17
64.	Annealing of Olin 907-17 for cryogenic DRIE in vacuum Heraeus convection furnace at 150°C, time>15 min
65.	Etching of Si Plasma OXFORD Oxford Plasma lab 100 ICP Basic recipes for deep trenches and through wafer etching
66.	Stripping of Olin 907 by oxygen plasma

Mask information

Mask Number	Description	Abbr.	INSIDE
O	Mask zero (mask mark)	M0	Dark
I	Photo-detector windows	PD	Clear
II	Shape of the channel	CH	Dark
III	First poly	PL1	Dark
IV	Antifuse windows	AW	Clear
V	Second poly	PL2	Dark
VI	Shaping separation nitride	SO	Dark
VII	Contact windows	CO	Clear
VIII	Metalization Aluminum	IN	Dark
IX	Channel end opening	EO	Clear
X	Shadow mask, liquid confinement	SM1	Clear
XI	Shadow mask, reserved solution	SM2	Clear

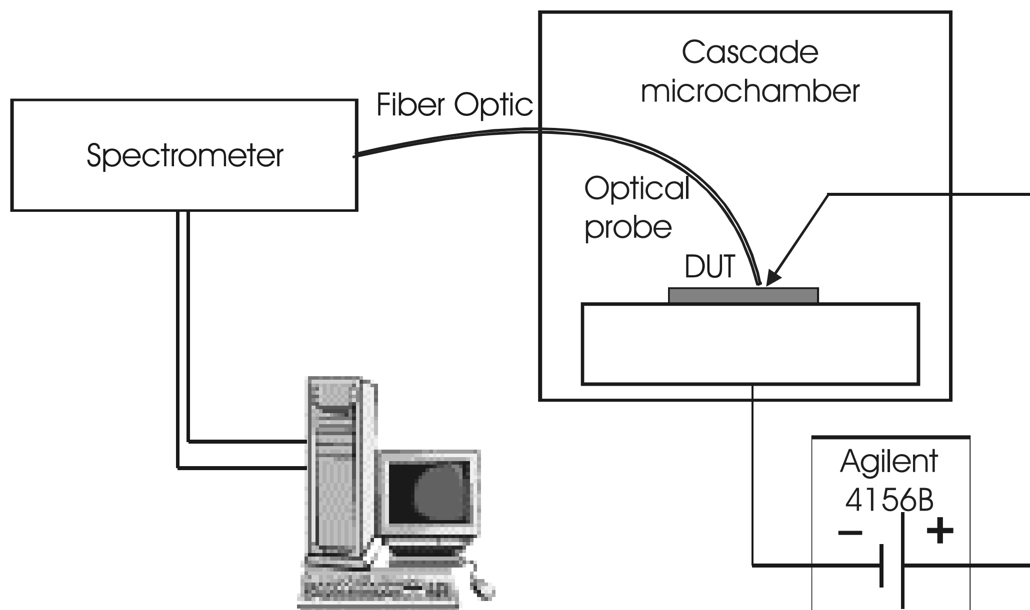
APPENDIX B

FORMULAS & CONSTANTS

Conversion between I(λ) [W/nm] & I(E) [W/eV]	$I(E)=10^{-9}\frac{\lambda^2}{hc}I(\lambda)$
Conversion of photon energy [eV] and wavelength [nm]	$\lambda=\frac{hc}{E}=10^3\frac{1.239}{E}$
Effective density of states in conduction band, N_C [cm^{-3}]	2.8×10^{19}
Effective density of states in valence band, N_V [cm^{-3}]	1.04×10^{19}
Fermi-Dirac distribution	$f(E)=\frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)}$
Optical phonon energy in Si [eV]	0.063
Refractive index of Si at 1120 nm (1.12 eV)	3.353
Si bandgap at 300K [eV]	1.1246
Temperature dependence of Si bandgap [eV]	$E(T)=E_o-\frac{\alpha T^2}{T+\beta}$ $E_o=1.170;\alpha=4.73\times10^{-4},\beta=636$
Thermal voltage at 300K [V]	$\frac{kT}{q}=0.0259$

APPENDIX C

THE SPECTROSCOPIC MEASUREMENT SETUP



This spectroscopic setup was used for measurements in chapter V, VI, and VII of the thesis.

For electrical measurements and supply, an Agilent 4156B/C precision parameter analyzer was used.

The emitted photons are collected from the front side window of the device with a fiber optical probe. Light emission spectra are measured from the output of the optical fiber with an Instrument Systems Spectro-320 universal spectrometer (http://www.instrument-systems.de/details/det_sp.htm) and/or an Avantes AVS-SD2000 spectrometer (http://www.avantes.com/downloads/AVACAT-SPEC.PDF).

LIST OF PUBLICATIONS

Journal Articles

Modeling of Light Emission from Silicon Nanometer-scale Diode antifuses
N. Akil, V. E. Houtsma, **P. LeMinh**, J. Holleman, V. Zieren, D. de Mooij, P. H. Woerlee, A. van den Berg, and H. Wallinga
Journal of Applied Physics, Vol. **88**(4), 2000.

Novel Integration of Microchannel with Silicon Light Emitting Diode-Antifuse
P. LeMinh, J. Holleman, H. Wallinga, J.W. Berenschot, N.R. Tas, and A. van den Berg
Submitted for publication in Journal of Micromechanics and Microengineering, IOP, 2003

Conference Articles

Visible Light Emission from Reverse-Biased Silicon Nanometer-scale Diode-Antifuses
V. E. Houtsma, J. Holleman, N. Akil, **P. LeMinh**, V. Zieren, A. van den Berg, H. Wallinga, and P. H. Woerlee
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Proceedings of the Transducer '01, pp. 544-547, Munich 2001.

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P. LeMinh, J. Holleman, H. Wallinga, and A. van den Berg
Proceedings of the 1st International Conference on Materials Processing for Properties and Performance (MP3), Singapore, 2002.

Highly Efficient Silicon Light Emitting Diode
P. LeMinh, J. Holleman, and H. Wallinga
Proceedings of the 5th SAFE on CD-ROM, Netherlands, 2002

BIOGRAPHY

Lê Minh Phương, called Phương, was born on the 30th, October 1974 in Hanoi. Having finished high school, he started his study in engineering physics at the Hanoi University of Technology (HUT) in 1991. Main subjects of his study were on physics of semiconductors, semiconductor devices and microelectronic technology. His practical term and graduation work were done at the MOS laboratory of the Institute of Engineering Physics. During this period, he worked on Spin-On-Glass (SOG) materials and technology for VLSI applications. In 1996, he received his engineer degree and started the master program of the International Training Institute for Materials Science (ITIMS). In 1998, he graduated as a Master of Engineering with the research on boron diffusion from SOG dopant source for making shallow p-n junctions. Thanks to the collaboration between ITIMS and the University of Twente, he was considered and consequently offered this PhD program at the Laboratory of Semiconductor Components (SC) of the Faculty of Electrical Engineering where he started in January 1999.

In his leisure time, Phương likes doing many sports such as swimming, playing football, snooker, ping-pong, chess… Besides, he is a very… talented poet of love and philosophy of life. Phương also has much interest in English; he used to teach English at two universities in Vietnam.